#### SDLS075

- Parallel Inputs and Outputs
- Four Operating Modes: Synchronous Parallel Load Right Shift Left Shift Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

түре	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
<b>'19</b> 4	36 MHz	195 mW
'LS194A	36 MHz	75 mW
<b>'</b> S194	105 MHz	425 mW

#### description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clock (do nothing) Shift right (in the direction  $Q_A$  toward  $Q_D$ ) Shift left (in the direction  $Q_D$  toward  $Q_A$ ) Parallel (broadside) load

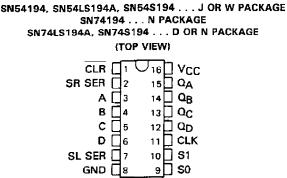
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when SO is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When SO is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

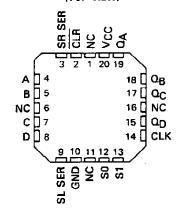
Clocking of the shift register is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

#### SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS March 1974-REVISED MARCH 1988

MARCH 1974-REVISED MARCH 1988

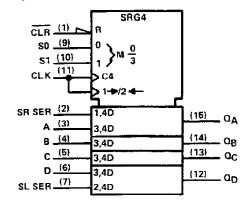


SN54LS194A, SN54S194 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D. J. N. and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications por the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.

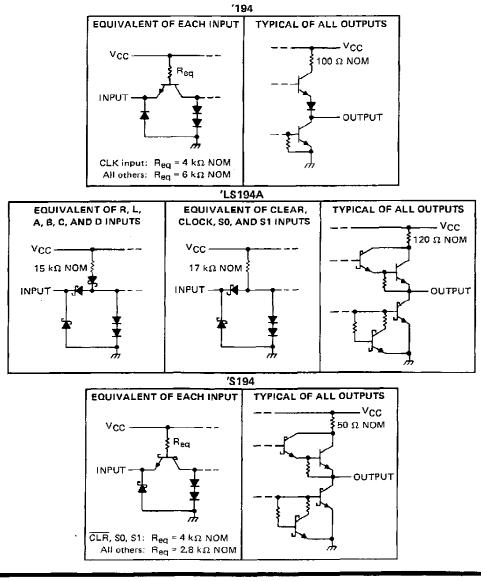


### SN54194, SN54LS194A, SN54S194 SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

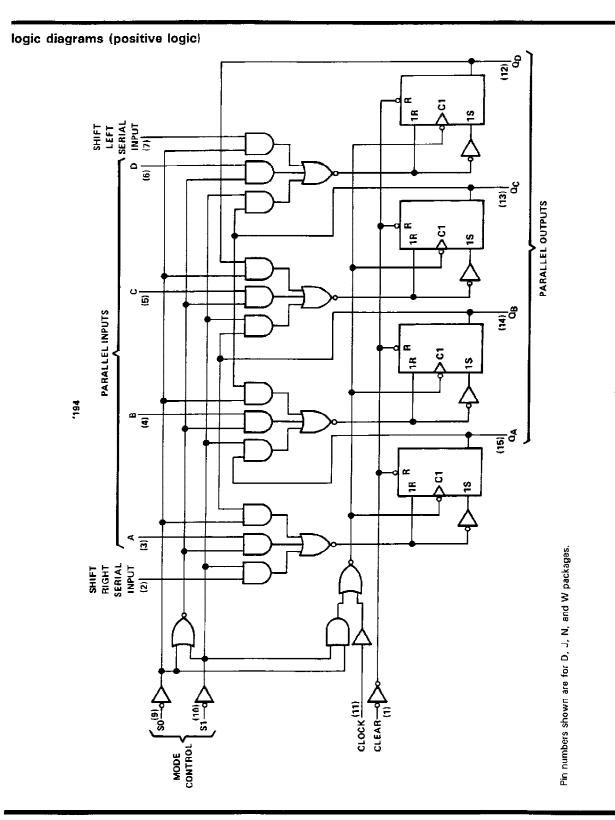
					FUNCTIO	N T	ABLE							
		_		INPUT	S						OUT	PUTS		Iн
	MC	DE		SE			PARA	LLE	L		~		0-	L
CLEAR	S1	SO	CLOCK	LEFT	RIGHT	Α	B	С	D	QA	QB	QC	QD	×
L	x	X	х	Х	х	X	х	х	х	L	L	L	L	t
н	х	х	L	x	x	X	х	х	х	Q <sub>A0</sub>	QB0	$Q_{CO}$	a <sub>D0</sub>	a.
н	н	н	1	x	х	a	b	c	d	а	b	с	đ	0
н	L	н	Ť	х	H.	X	х	х	×	н	Q <sub>Ап</sub>	Qgn	Q <sub>Cn</sub>	-
н	L	н	1	X	L	x	х	х	х	L	Q <sub>An</sub>	OBn	Q <sub>Сп</sub>	
н	н	L	†	н	х	x	х	х	х	QBn		a <sub>Dn</sub>	u	٩
н	н	L	1	L	х	x	х	х	х	QBn	QCn	QDu	L	-
н	L	L	×	x	х	х	х	х	х	QAO	OB0	$\mathbf{Q}_{\mathbf{CO}}$	QDO	1

- H = high level (steady state)
  - low level (steady state)
- X = irrelevant (any input, including tran-
- sitions)
- $\uparrow$  = transition from low to high level
- a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
- $Q_{AQ}, Q_{BQ}, Q_{CQ}, Q_{DQ} =$  the level of  $Q_A$ ,  $Q_B, Q_C$ , or  $Q_D$ , respectively, before the indicated steady-state input conditions were established.

#### schematics of inputs and outputs

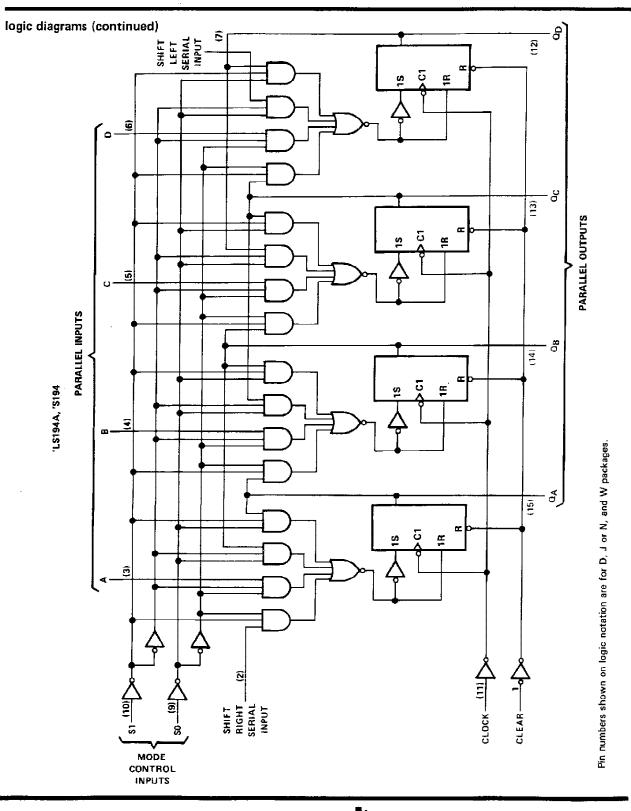






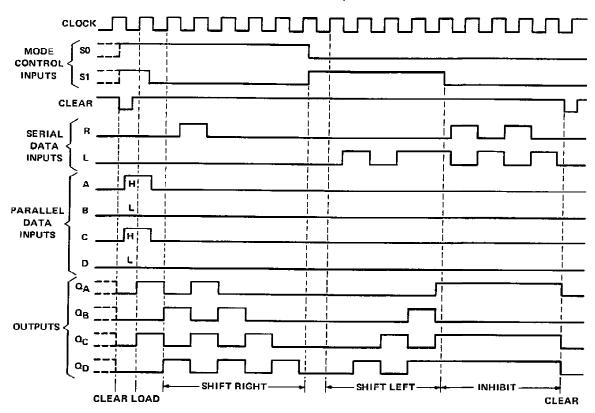
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# SN54LS194A, SN54S194 SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



TEXAS INSTRUMENTS

# SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



typical clear, load, right-shift, left-shift, inhibit, and clear sequences



### SN54194, SN74194 **4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V <sub>CC</sub> (see Note 1)	,			•		 								7 V
Input voltage														
Operating free-air temperature range: SN54194			: .								-Ę	55° (	C to	125°C
SN74194												0	°Cı	o 70°C
Storage temperature range						 •	•		•		-6	5°۵	C to	150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

			SN5419	4		SN7419	4	UNIT
		MIN	NÔM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-800			-800	μA
Low-level output current, IOL				16			16	mA
Clock frequency, fclock		0		25	0		25	MHz
Width of clock or clear pulse, tw		20			20			ns
	Mode control	30			30			ns
Setup time, t <sub>su</sub>	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t <sub>h</sub>		0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

_			uouziouot		SN5419	4		SN7419	4	
	PARAMETER	TEST CC	NDITIONS	MIN	түр‡	мах	MIN	TYP‡	MAX	UNIT
Vін	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	V
VIK	Input clamp voltage	V <sub>CC</sub> = MIN,	l₁ =12 mA			-1.5			-1.5	V
VOH	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V,	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -800 μA	2.4	3.4		2.4	3.4		v
Vol	Low-level output voltage	V <sub>CC</sub> = MIN, VIL = 0.8 V,	V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	v
Т <u>р</u>	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V1 = 5.5 V			1			1	mΑ
ΠН	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.4 V			40			40	μА
41	Low-level input current	V <sub>CC</sub> = MAX,	VI = 0.4 V			-1.6	_		-1.6	mA
los	Short-circuit output current §	V <sub>CC</sub> = MAX		-20		-57	-18		-57	mA
ICC	Supply current	V <sub>CC</sub> = MAX,	See Note 2		39	63		39	63	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ . §Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I<sub>CC</sub> is tested with a momentary GND, then 4.5 V applied to clock.

### switching characteristics, VCC = 5 V, TA = 25 °C

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
fmax	Maximum clock frequency	- C( = 15 pF,	25	36		MHz
TPHL	Propagation delay time, high-to-low-level output from clear	$- R_{I} = 400 \Omega_{r}$		19	30	ns
<b>tPLH</b>	Propagation delay time, low-to-high-level output from clock	- See Figure 1		14	22	ns
<b>tPHL</b>	Propagation delay time, high-to-low-level output from clock	Jee rigure i		17	26	ns

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## SN54LS194A, SN74LS194A 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) .											•			7 V
Input voltage														7 V
Operating free-air temperature range:														
	SN74LS194A	-		. ,								0°C	to 7	0°C
Storage temperature range			•				-		٠	•	-65	δ°C t	o 15	О°С
 a tatan a tahun una ara-														

NOTE 1: Voltage values are with respect to network ground terminal,

#### recommended operating conditions

	··· · · · ·	SN	54LS19	4A	SN	74LS19	4A	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	<b>_</b>			-400			-400	μA
Low-level output current, IOL	······································	1		4	1		8	mA
Clock frequency, fclock		0		25	0		25	MHz
Width of clock or clear pulse, tw		20			20			กร
	Mode control	30			30			D5
Setup time, t <sub>su</sub>	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			п5
Hold time at any input, <sup>t</sup> h		0			0			ns
Operating free-air temperature, TA		55		125	0		70	°Ċ

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TE	T CONDUTI		SN	54LS19	4A	SN	74LS19	4A	
	High-level output voltage $V_{CC} = MIN$ , $V_{IH} = 2 V$ , $V_{IL} = V_{IL} max$ , $I_{OH} = -400$ $V_{CC} = MIN$ , $V_{IH} = 2 V$ , $V_{IL} = V_{IL} max$ , $I_{OH} = -400$ $V_{CC} = MIN$ , $V_{IH} = 2 V$ , $V_{IH} = 2 V$ , $V_{IL} = V_{IL} max$ Input current at maximum input voltage $V_{CC} = MAX$ , $V_{I} = 7 V$ High-level input current $V_{CC} = MAX$ , $V_{I} = 2.7 V$ Low-level input current $V_{CC} = MAX$ , $V_{I} = 0.4 V$	2NS -	MIN	TYP	MAX	MIN	TYP‡	MAX	UNIT		
VIH	High-level input voltage	1			2			2			V
VIL	Low-level input voltage						0.7			0.8	Γv Ι
٧ı	Input clamp voltage	V <sub>CC</sub> = MIN,	lı ≃ —18 mA	· · · · · · · · · · · · · · · · · · ·	1		-1.5			-1.5	· V
۷он	High-level output voltage		•••	μA	2.5	3.5		2.7	3.5		v
		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	1 <sub>0L</sub> = 4 mA		0.25	0.4	<u> </u>	0.25	0.4	v
YOL		VIL = VIL max		IOL = 8 mA					0.35	0.5	l v
4	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 7 V				0.1			0.1	mA
Чн	High-level input current	V <sub>CC</sub> = MAX,	VI = 2.7 V				20			20	μA
μL	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V				-0,4			-0.4	ΜA
los	Short-circuit output current §	V <sub>CC</sub> = MAX			-20		-100	-20		-100	mΑ
lcc	Supply current	V <sub>CC</sub> = MAX,	See Note 2		1	15	23		15	23	mΑ

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I<sub>CC</sub> is tested with a momentary GND, then 4.5 V, applied to clock.

### switching characteristics, $V_{CC} = 5 V$ , $T_A = 25 °C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	- CL = 15 pF,	25	36		MHz
<b>tPHL</b>	Propagation delay time, high-to-low-level output from clear	- CL ≃ rope, - Ri ≃ 2 kΩ,		19	30	ns
<sup>t</sup> PLH	Propagation delay time, low-to-high level output from clock	See Figure 1		14	22	វាន
<b>t</b> PHL	Propagation delay time, high to low level output from clock	See Figure 5		17	26	ns

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## SN54S194, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V <sub>CC</sub> (see Note 1)			-																7V
Input voltage		•			•														5.5V
Operating free-air temperature range:	SN54S194		-	-	-	-							-	-					–55°C to 125°C
	SN74S194											•				•			. 0°C to 70°C
Storage temperature range		•	٠	•	•	• •	•••	•	• •	•	•	•	•	•	•	•	·	-	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

		5	SN5451	94	5	SN74S19	94	l
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	<u>_</u>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH		1		-1	· · · ·		1	mA
Low-level output current, IOL		1		20	<b>—</b>		20	mA
Clock frequency, fclock		0		70	0		70	MHz
Width of clock pulse, tw(clock)		7			7	•		ns
Width of clear pulse, tw(clear)		12			12			ns
	Mode control	11	_		11			ns
Setup time, t <sub>su</sub>	Serial and parallel data	5			5			пѕ
	Clear inactive-state	9			9			ns
Hold time at any input, t <sub>h</sub>	····	3			3			ns
Operating free-air temperature, TA		-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[	PARAMETER	TEST CONDITIONS <sup>†</sup>	5	SN54S <u>1</u> S	14	5	34		
i		TEST CONDITIONS	MIN	TYP <sup>‡</sup>	MAX	MIN	ТҮР‡	MAX	UNIT
Ин	High-level input voltage		2			2			v
VIL	Low-level input voltage		1		0.8		·	0.8	V
Viк	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>1</sub> =18 mA	1		-1.2			-1.2	V
∨он	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = -1 mA	2,5	3.4		2.7	3.4		v
Vol	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA			0.5			0.5	v
1	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>1</sub> = 5.5 V	1		1			1	mA
ίн	High-level input current	V <sub>CC</sub> = MAX, V <sub>1</sub> = 2.7 V	<u> </u>		50	<b></b>		50	μA
1L	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V		-	-2	-		2	mA
los	Short-circuit output current§	V <sub>CC</sub> = MAX	-40		-100	-40		-100	mA
		VCC = MAX, See Note 2	1	85	135		85	135	-
lcc	Supply current	V <sub>CC</sub> = MAX, T <sub>A</sub> = 125°C, W package See Note 2			110				mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

 ${
m \$}$  Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applies to S0, S1, clear, and the serial inputs, I<sub>CC</sub> is tested with a momentary GND, then 4.5 V, applied to clock.

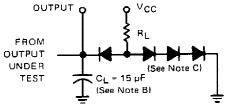
### switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25 °C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	0 - 15 -5	70	106		MHz
<b>t</b> PHL	Propagation delay time, high-to-low-level output from clear	- CL ≈ 15 pF,		12.5	18.5	ns
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output from clock	$R_{L} = 280 \Omega,$	4	8	12	n\$
TPHL	Propagation delay time, high-to-low-level output from clock	See Figure 1	4	11	16.5	ns



## SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

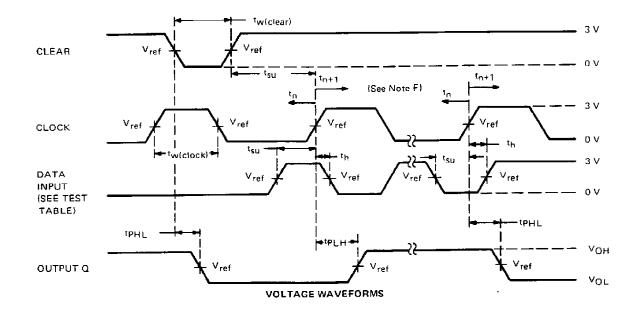
#### PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

. TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT			OUTPUT TESTED
FOR TEST	S1	<b>S</b> 0	(SEE NOTE E)
A	4.5 V	4.5 V	Ω <sub>A</sub> at t <sub>n+1</sub>
В	4.5 V	4.5 V	QB at tn+1
с	4.5 V	4.5 V	QC at tn+1
D	4.5 V	4.5 V	QD at tn+1
L Serial Input	4.5 ∨	0 V	Q <sub>A</sub> at t <sub>n+4</sub>
R Serial Input	٥v	4.5 V	Q <sub>D</sub> at t <sub>n+4</sub>



NOTES: A. The clock pulse generator has the following characteristics:  $Z_{out} \approx 50 \Omega$  and PRR  $\leq$  1 MHz, For '194,  $t_r \leq$  7 ns and  $t_f \leq$  7 ns. For 'LS194A,  $t_r \leq$  15 ns and  $t_f \leq$  6 ns. For 'S194,  $t_r \leq$  2.5 ns and  $t_f \leq$  2.5 ns. When testing f<sub>max</sub>, vary PRR.

- B. C<sub>1</sub> includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. A clear pulse is applied prior to each test.
- E. For '194 and 'S194,  $V_{ref}$  = 1.5 V; for 'LS194A,  $V_{ref}$  = 1.3 V.
- F. Propagation delay times (tpLH and tpHL) are measured at tn+1. Proper shifting of data is verified at tn+4 with a functional test.
- G.  $t_n = bit time before clocking transition.$ 
  - $t_{n+1}$  = bit time after one clocking transition.  $t_{n+4}$  = bit time after four clocking transitions.

FIGURE 1-SWITCHING TIMES





25-Sep-2013

# **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
7604001EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604001EA SNJ54S194J	Samples
7604001FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604001FA SNJ54S194W	Samples
7604001FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604001FA SNJ54S194W	Samples
JM38510/07601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BEA	Samples
JM38510/07601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BEA	Samples
JM38510/07601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BFA	Samples
JM38510/07601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BFA	Samples
JM38510/30601B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30601B2A	Samples
JM38510/30601B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30601B2A	Samples
JM38510/30601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BEA	Samples
JM38510/30601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BEA	Samples
JM38510/30601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BFA	Samples
JM38510/30601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BFA	Samples
M38510/07601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BEA	Samples
M38510/07601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BEA	Samples
M38510/07601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BFA	Samples
M38510/07601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07601BFA	Samples



# PACKAGE OPTION ADDENDUM

25-Sep-2013

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Sampl
M38510/30601B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30601B2A	Samp
M38510/30601B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30601B2A	Sampl
M38510/30601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BEA	Sampl
M38510/30601BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BEA	Samp
M38510/30601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BFA	Samp
M38510/30601BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30601BFA	Samp
SN54194J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN54194J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN54LS194AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS194AJ	Samp
SN54LS194AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS194AJ	Samp
SN54S194J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S194J	Samp
SN54S194J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S194J	Samp
SN74194N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74194N	OBSOLETE	E PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS194AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS194A	Samj
SN74LS194AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS194A	Samp
SN74LS194ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS194A	Samj
SN74LS194ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS194A	Samj
SN74LS194ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS194A	Samj
SN74LS194ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS194A	Samj



# PACKAGE OPTION ADDENDUM

25-Sep-2013

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Sample
SN74LS194AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS194AN	Sample
SN74LS194AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS194AN	Sample
SN74LS194AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS194AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS194ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS194AN	Sample
SN74LS194ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS194AN	Sample
SN74S194N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S194N	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	0 to 70		
SN74S194N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	0 to 70		
SN74S194N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	0 to 70		
SNJ54LS194AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 194AFK	Sample
SNJ54LS194AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 194AFK	Sample
SNJ54LS194AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS194AJ	Sample
SNJ54LS194AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS194AJ	Sample
SNJ54LS194AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS194AW	Sample
SNJ54LS194AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS194AW	Sample
SNJ54S194FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 194FK	Sample
SNJ54S194FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 194FK	Sample
SNJ54S194J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604001EA SNJ54S194J	Sample
SNJ54S194J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604001EA SNJ54S194J	Sample
SNJ54S194W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604001FA SNJ54S194W	Sample



25-Sep-2013

Orderable Device	Status	Package Typ	e Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
SNJ54S194W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604001FA SNJ54S194W	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(<sup>5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 :

• Catalog: SN74194, SN74LS194A, SN74S194



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# PACKAGE OPTION ADDENDUM

25-Sep-2013

• Military: SN54194, SN54LS194A, SN54S194

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

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