

DM74ALS74A Dual D Positive-Edge-Triggered Flip-Flop with Preset and Clear

General Description

The 'ALS74A contains two independent positive edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{\mathbf{Q}}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

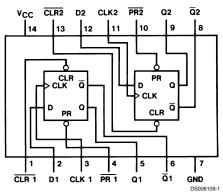
Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over LS74 at approximately half the power

Connection Diagram

Dual-In-Line Package



Order Number DM74ALS74AM, DM74ALS74AN or DM74ALS74ASJ See Package Number M14A, M14D or N14A

Function Table

Inputs				Outputs		
PR	CLR	CLK	D	Q	Q	
L	Н	Х	Х	Н	L	
Н	L	Χ	X	L	Н	
L	L	X	X	H (Note 1)	H (Note 1)	
Н	Н	1	Н	Н	L	
Н	Н	1	L	L	Н	
Н	Н	L	Χ	Q_{o}	\overline{Q}_{o}	

Note 1: This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Absolute Maximum Ratings (Note 2)

Supply Voltage 7V Input Voltage 7V

Operating Free Air Temperature Range

DM74ALS 0° C to +70 $^{\circ}$ C

Storage Temperature Range

-65°C to +150°C

Typical θ_{JA}

N Package M Package 87.0°C/W 117.0°C/W

Recommended Operating Conditions

Symbol	Parameter		DM7	Units		
		Min	Nom	Max		
V _{cc}	Supply Voltage		4.5	5	5.5	V
V _{IH}	High Level Input Voltage		2			V
V _{IL}	Low Level Input Voltage				0.8	V
I _{OH}	High Level Output Current				-0.4	mA
I _{OL}	Low Level Output Current				8	mA
f _{CLK}	Clock Frequency		0		34	MHz
t _{W(CLK)}	Width of Clock Pulse	High	14.5			ns
		Low	14.5			ns
t _W	Pulse Width	Low	14.5			ns
	Preset & Clear					
t _{SU}	Data Setup Time	Data	15↑ (Note 3)			
		PRE or CLR	10↑ (Note 3)			ns
		Inactive				
t _H	Data Hold Time	•	0↑ (Note 3)			ns
T _A	Free Air Operating Temperature		0		70	°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

	, ,		* *	00 / //			
Symbol	Parameter	Conditions		Min	Тур	Max	Units
V _{IK}	Input Clamp Voltage	V _{CC} = 4.5V, I _I =	= –18 mA			-1.5	V
V _{OH}	High Level Output	$I_{OH} = -0.4 \text{ mA}$		V _{CC} - 2			V
	Voltage	$V_{CC} = 4.5V \text{ to } 5$	5.5V				
V _{OL}	Low Level Output	V _{CC} = 4.5V	74ALS		0.35	0.5	V
	Voltage	V _{IH} = 2V	$I_{OL} = 8 \text{ mA}$				
I _I	Input Current @	V _{CC} = 5.5V,	Clock, D			0.1	mA
	Max Input Voltage	V _{IH} = 7V	Preset, Clear			0.2	
I _{IH}	High Level	$V_{CC} = 5.5V,$	Clock, D			20	μA
	Input Current	V _{IH} = 2.7V	Preset, Clear			40	
I _{IL}	Low Level	V _{CC} = 5.5V,	Clock, D			-0.2	mA
	Input Current	$V_{IL} = 0.4V$	Preset, Clear			-0.4	
Io	Output Drive Current	V _{CC} = 5.5V, V _O	$V_{CC} = 5.5V, V_{O} = 2.25V$			-112	mA
I _{cc}	Supply Current	V _{CC} = 5.5V (No	te 4)		2.4	4	mA

 $[\]textbf{Note 4: } I_{\text{CC}} \text{ is measured with D, CLK and PRESET grounded, then with D, CLK and CLEAR grounded.}$

Note 3: The (↑) arrow indicates the positive edge of the Clock is used for reference.

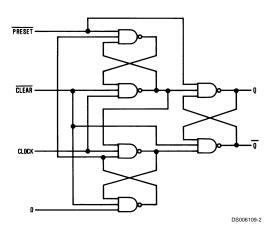
Note 5: $I_{\rm IL}$ PRE and CLR pins not guaranteed to meet specifications with both PRE and CLK low.

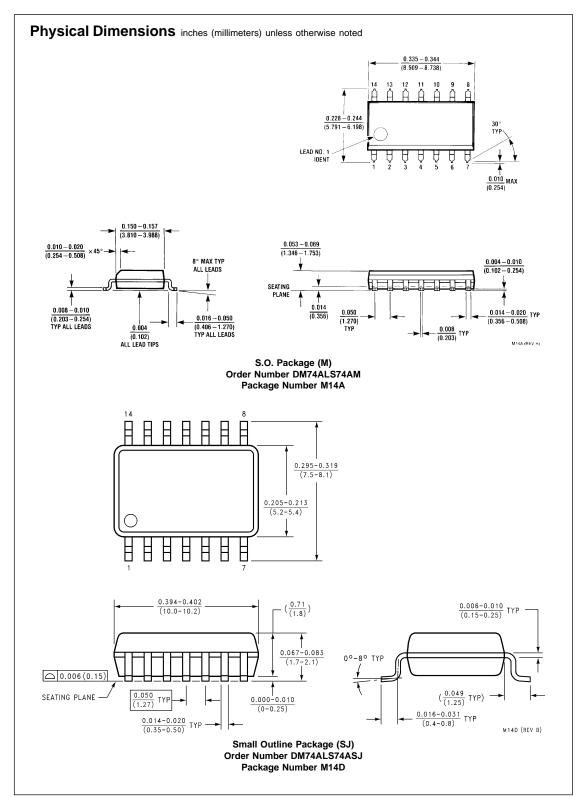
Switching Characteristics over recommended operating free air temperature range. (Note 6)

Parameter	Conditions	From	То	DM74ALS74A		Units
				Min	Max	
f _{MAX}	V _{CC} = 4.5V to 5.5V			34		MHz
t _{PLH}	$R_L = 500\Omega$	Preset	Q or Q	3	13	ns
t _{PHL}	C _L = 50 pF	or Clear		5	15	ns
t _{PLH}		Clock	Q or Q	5	16	ns
t _{PHL}				5	18	ns

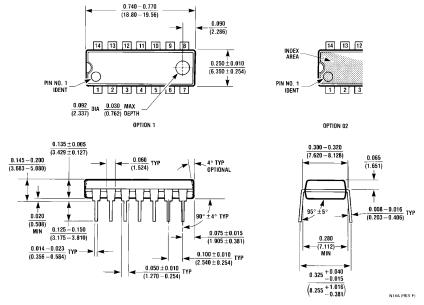
Note 6: See Section 1 for test waveforms and output load.

Logic Diagram





Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N) Order Number DM74ALS74AN Package Number N14A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DE-VICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMI-CONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation Americas Customer Response Center

Tel: 1-888-522-5372

Fairchild Semiconductor Europe

Fax: +49 (0) 1 80-530 85 86 Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd. 13th Floor, Straight Block Ocean Centre, 5 Canton Rd.

Tsimshatsui, Kowloon Hong Kong Tel: +852 2737-7200 Fax: +852 2314-0061 National Semiconductor Japan Ltd. Tel: 81-3-5620-6175 Fax: 81-3-5620-6179

www.fairchildsemi.com