QUAD 2-INPUT EXCLUSIVE-OR GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT86 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT86 provide the EXCLUSIVE-OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/$ t_{PLH}	propagation delay nA, nB to nY	$C_L = 15\,pF$ $V_{CC} = 5\,V$	11	14	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	30	pF

GND = 0 V; $T_{amb} = 25\,°C$; $t_r = t_f = 6$ ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\ (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz $\quad C_L$ = output load capacitance in pF
   f_o = output frequency in MHz $\quad V_{CC}$ = supply voltage in V
   $\Sigma\ (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC   the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5\ V$

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27)
14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

Fig. 1 Pin configuration.

Fig. 2 Logic symbol.

Fig. 3 IEC logic symbol.
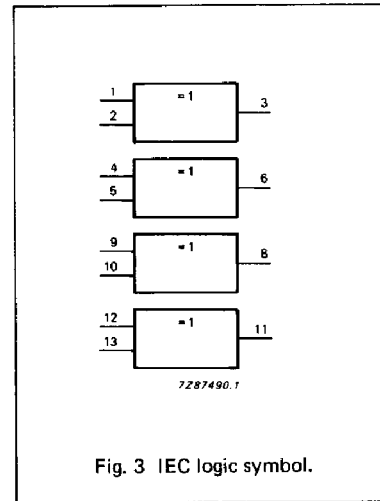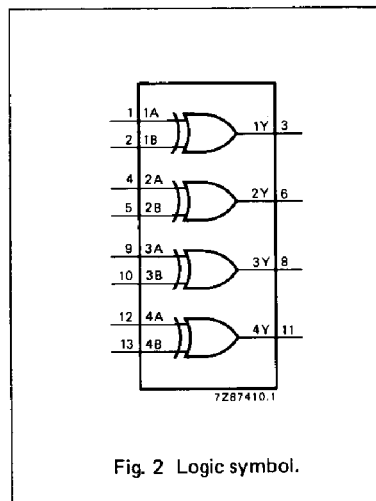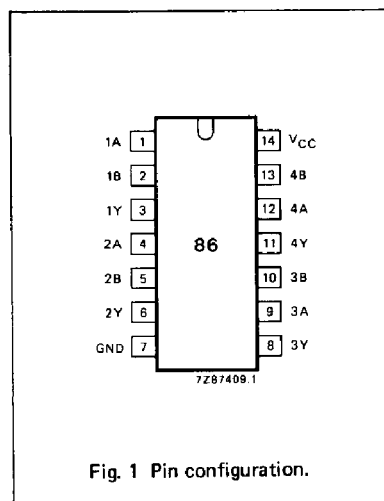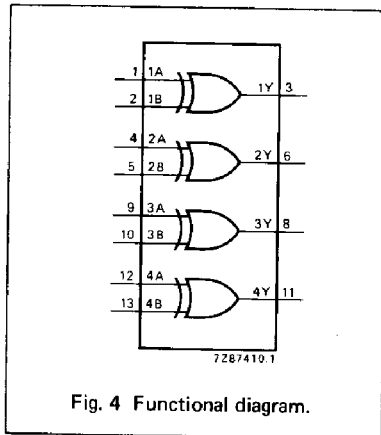
Fig. 4 Functional diagram.
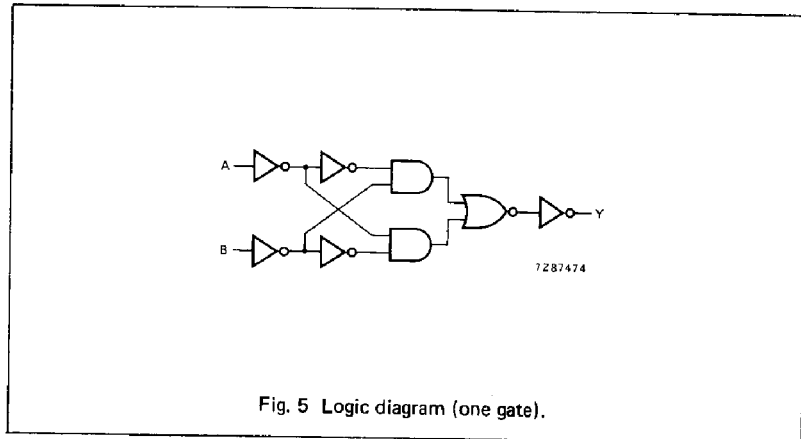
Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC						UNIT	TEST CONDITIONS	
		+25			−40 to +85	−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/$ t_{PLH}	propagation delay nA, nB to nY		17	32		40		48	ns	4.5	Fig. 6
$t_{THL}/$ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.
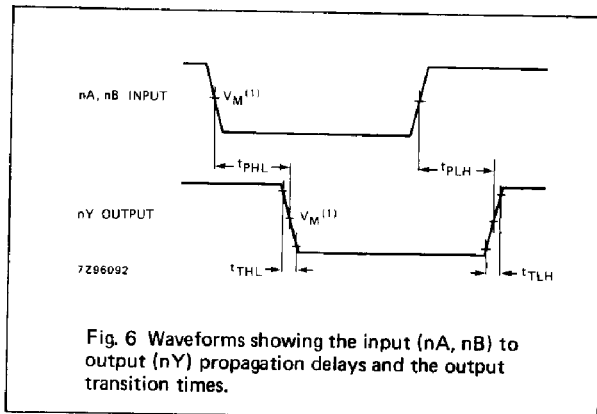
Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = $ GND to V_{CC}.
    HCT: $V_M = 1.3$ V; $V_I = $ GND to 3 V.