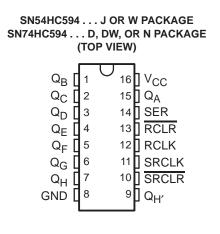
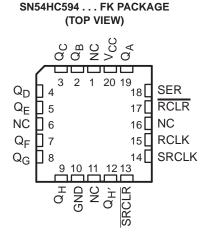
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 15 ns
- ±6-mA Output Drive at 5 V



- Low Input Current of 1 μA Max
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage

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- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers



NC - No internal connection

description/ordering information

The 'HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (\overline{RCLR} , \overline{SRCLR}) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

The parallel $(Q_A - Q_H)$ outputs have high-current capability. $Q_{H'}$ is a standard output.

TA	PACKA	GEŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HC594N	SN74HC594N
		Tube of 40	SN74HC594D	
4000 to 0500	SOIC – D	Reel of 2500	SN74HC594DR	HC594
–40°C to 85°C		Reel of 250	SN74HC594DT	
		Tube of 40	SN74HC594DW	110504
	SOIC – DW	Reel of 2000	SN74HC594DWR	HC594
	CDIP – J	Tube of 25	SNJ54HC594J	SNJ54HC594J
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC594W	SNJ54HC594W
	LCCC – FK	Tube of 55	SNJ54HC594FK	SNJ54HC594FK

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS SCLS040F – DECEMBER 1982 – REVISED OCTOBER 2003

	FUNCTION TABLE								
		INPUTS			FUNCTION				
SER	SRCLK	SRCLR	RCLK	RCLR	FUNCTION				
Х	Х	L	Х	Х	Shift register is cleared.				
L	Ŷ	Н	Х	х	First stage of shift register goes low. Other stages store the data of previous stage, respectively.				
н	\uparrow	Н	Х	х	First stage of shift register goes high. Other stages store the data of previous stage, respectively.				
L	\downarrow	Н	Х	Х	Shift register state is not changed.				
Х	Х	Х	Х	L	Storage register is cleared.				
Х	Х	Х	\uparrow	Н	Shift register data is stored in the storage register.				
Х	Х	Х	\downarrow	Н	Storage register state is not changed.				



RCLR 13 12 RCLK -10 SRCLR -11 SRCLK R 3R 14 SER -15 Q_A 1D > C1 > C3 C 0 R 3S 2S R 2R 3R 1 - Q_B > C2 > C3 C R 3S 2S R 2R 3R 2 – Q_C > C2 **> C3** \cap R 3S 2S R 2R 3R 3 - Q_D > C2 > C3 \cap R 3S 2S R \odot 2R 3R 4 QE > C2 > C3 R 3S R 2S (5 QF 3R 2R > C2 -0 > C3 R 3S R 2S \cap 2R 3R 6 - QG > C3 > C2 R 3S R 2S Ċ 2R 3R 7 - Q_H > C2 > C3 R 3S 9 - Q_H′

logic diagram (positive logic)

Pin numbers shown are for the D, DW, J, N, and W packages.



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timing diagram

SRCLK	
SER	
RCLK	
SRCLR	
RCLR	
Q _A	
QB	
QC	
QD	
QE	
QF	
QG	
QH	
Q _{H′}	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		
Input clamp current, I_{IK} (V _I < 0 or V _I > V _{CC}) (s		
Output clamp current, I_{OK} (V _O < 0 or V _O > V _C		
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$		
Continuous current through V _{CC} or GND		
Package thermal impedance, θ_{JA} (see Note 2)		
		57°C/W
	N package	
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions (see Note 3)

			SN	154HC59	94	SN74HC594			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	2	5	6	V
		$V_{CC} = 2 V$	1.5			1.5			
VIH High-level input voltage		$V_{CC} = 4.5 V$	3.15		2	3.15			V
	$V_{CC} = 6 V$	4.2		54	4.2				
		$V_{CC} = 2 V$		ĨEL	0.5			0.5	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$		2	1.35			1.35	V
		ACC = 6 A		5	1.8			1.8	
VI	Input voltage		0	2	VCC	0		VCC	V
VO	Output voltage		0		V _{CC}	0		VCC	V
		$V_{CC} = 2 V$			1000			1000	
t _t Input	Input transition (rise and fall) time	$V_{CC} = 4.5 V$			500			500	ns
		ACC = 6 A			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				Т	A = 25°C	;	SN54H	IC594	SN74H	C594	
PARAMETER	IES	CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
VOH	$V_I = V_{IH} \text{ or } V_{IL}$	$Q_{H'}, I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		V
		$Q_A - Q_H$, $I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$Q_{H'}$, I_{OH} = -5.2 mA	6 V	5.48	5.8		5.2	EW	5.34		
		Q_A-Q_H , $I_{OH} = -7.8$ mA	6 V	5.48	5.8		5.2	EN	5.34		
			2 V		0.002	0.1	4	0.1		0.1	
		I _{OL} = 20 μA	4.5 V		0.001	0.1	رى د	0.1		0.1	
			6 V		0.001	0.1	201	0.1		0.1	
VOL	$V_I = V_{IH} \text{ or } V_{IL}$	$Q_{H'}, I_{OL} = 4 \text{ mA}$	45.1		0.17	0.26	PPC	0.4		0.33	V
		$Q_A - Q_H$, $I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26	1	0.4		0.33	
		Q _{H'} , I _{OL} = 5.2 mA			0.15	0.26		0.4		0.33	
		Q_A-Q_H , $I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
Ц	$V_I = V_{CC} \text{ or } 0$		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	$V_{O} = V_{CC} \text{ or } 0$		6 V		±0.01	±0.5		±10		±5	μΑ
Icc	$V_I = V_{CC} \text{ or } 0,$	l _O = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				T _A =	25°C	SN54F	IC594	SN74H	IC594	
			Vcc	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		5		3.3		4	
fclock	Clock frequency		4.5 V		25		17		20	MHz
			6 V		29		20		24	
			2 V	100		150		125		
		SRCLK or RCLK high or low	4.5 V	20		30		25		
	B I I <i>I</i>		6 V	17		25		21		
tw	Pulse duration		2 V	100		150		125		ns
		SRCLR or RCLR low	4.5 V	20		30		25		
			6 V	17		25		21		
			2 V	90		135	2	110		
		SER before SRCLK↑	4.5 V	18		27	VIE	22		
		6 V	15		23	RE	19			
		2 V	90		135	. <i>K</i>	110			
		SRCLK↑ before RCLK↑†	4.5 V	18		27		22		
			6 V	15		23		19		
			2 V	50		Q 75		63		
t _{su}	Setup time	SRCLR low before RCLK1	4.5 V	10		15		13		ns
			6 V	9		13		11		
			2 V	20		20		20		
		SRCLR high (inactive) before SRCLK↑	4.5 V	10		10		10		
			6 V	10		10		10		
			2 V	5		5		5		
		RCLR high (inactive) before SRCLK↑	4.5 V	5		5		5		
			6 V	5		5		5		
			2 V	5		5		5		
^t h	Hold time, SER a	fter SRCLK↑	4.5 V	5		5		5		ns
				5		5		5		

[†]This setup time ensures that the output register receives stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.



SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS SCLS040F – DECEMBER 1982 – REVISED OCTOBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

	FROM	то		T,	α = 25°C	*	SN54H	IC594	SN74F	IC594	
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	5	8		3.3		4		
fmax			4.5 V	25	35		17		20		MH
			6 V	29	40		20		24		
			2 V		50	150		225		185	
SRCLK	Q _H ′	4.5 V		20	30		45		37		
			6 V		15	25		38		31	
^t pd			2 V		50	150		225		185	ns
	RCLK	$Q_A - Q_H$	4.5 V		20	30		45		37	
			6 V		15	25	4	2 38		31	
	SRCLR		2 V		50	150	(C)	225		185	
		Q _{H′}	Q _H ′	4.5 V		20	30	20	45		37
touu			6 V		15	25	40	38		31	ns
^t PHL			2 V		50	125	7	185		155	113
	RCLR	$Q_A - Q_H$	4.5 V		20	25		37		31	
			6 V		15	21		31		26	
			2 V		38	75		110		95	
		Q _H ′	4.5 V		8	15		22		19	
tt			6 V		6	13		19		16	ns
-i			2 V		38	60		90		75	
		Q _A –Q _H	4.5 V		8	12		18		15	
			6 V		6	10		15		13	

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

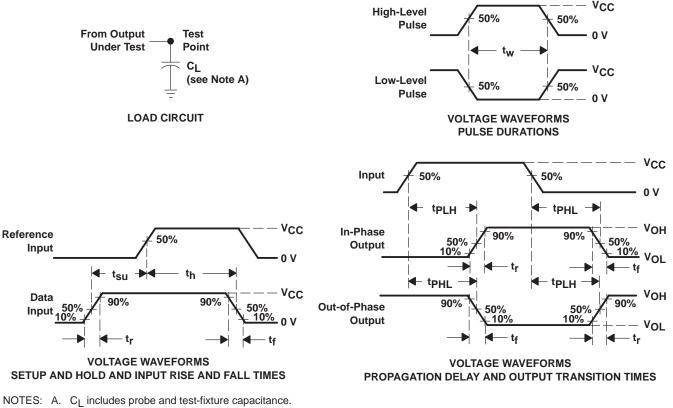
DADAMETED	FROM	то	V	Т	₄ = 25°C	;	SN54HC	594	SN74H	IC594	
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		90	200		300		250	
^t pd	RCLK	Q _A –Q _H	4.5 V		23	40		60		50	ns
·			6 V		19	34		51		43	
			2 V		90	200	00	300		250	
^t PHL	RCLR	Q _A -Q _H	4.5 V		23	40	c,	60		50	ns
			6 V		19	34	70	51		43	
			2 V		45	210	4	315		265	
tt		Q _A –Q _H	4.5 V		17	42		63		53	ns
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	395	pF



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PARAMETER MEASUREMENT INFORMATION

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_{O} = 50 $\Omega,$ t_{f} = 6 ns, t_{f} = 6 ns.
- C. For clock inputs, fmax is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tPLH and tPHL are the same as tpd.
- F. t_f and t_r are the same as t_t .

Figure 1. Load Circuit and Voltage Waveforms



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18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HC594D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC594N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC594NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame



retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

1	All dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ĺ	SN74HC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ſ	SN74HC594DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

21-Jan-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC594DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC594DWR	SOIC	DW	16	2000	366.0	364.0	50.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/D 06/11

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 Example 2,00 Solder Mask Opening

(See Note E)

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

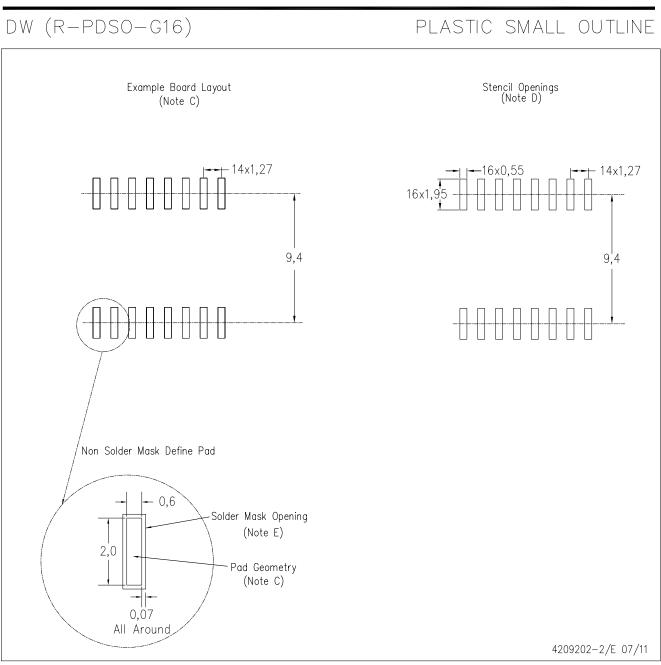
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AA.



LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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