SLLS115B – OCTOBER 1980 – REVISED MAY 1995

- **AM26LS32A Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and ITU Recommendations V.10 and V.11**
- **AM26LS32A Has ±7-V Common-Mode Range With ±200-mV Sensitivity**
- **AM26LS32A Has ±15-V Common-Mode Range With ±500-mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operates From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output Enable Inputs**
- **Input Impedance . . . 12 kΩ Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32™ and AM26LS33™**

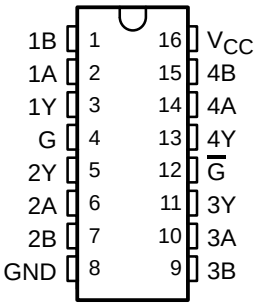
description

The AM26LS32A and AM26LS33A are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection direct to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

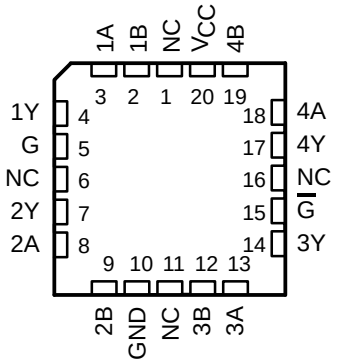
Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and AM26LS33AM are characterzed for operation over the full military temperature range of –55°C to 125°C.

AM26LS32AC, AM26LS33AC . . . D OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

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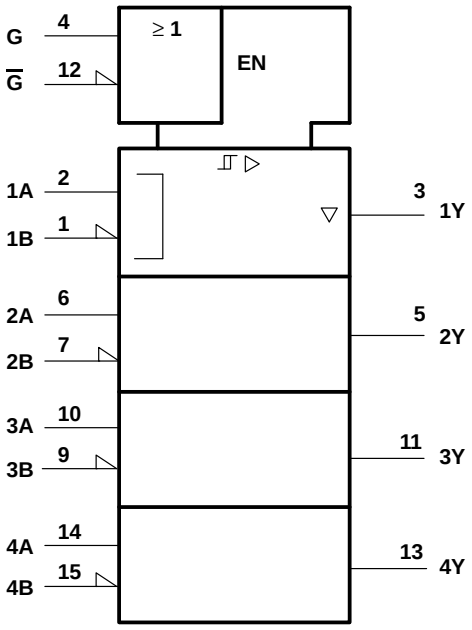
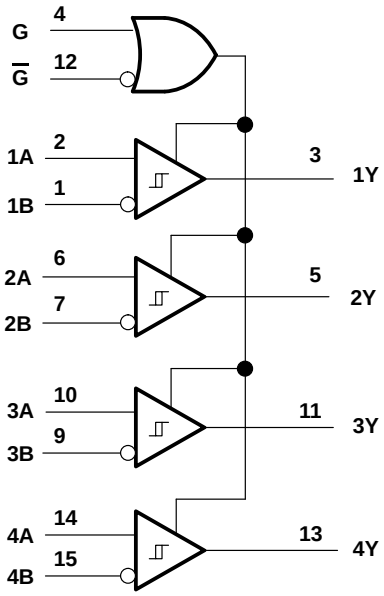
logic symbol†

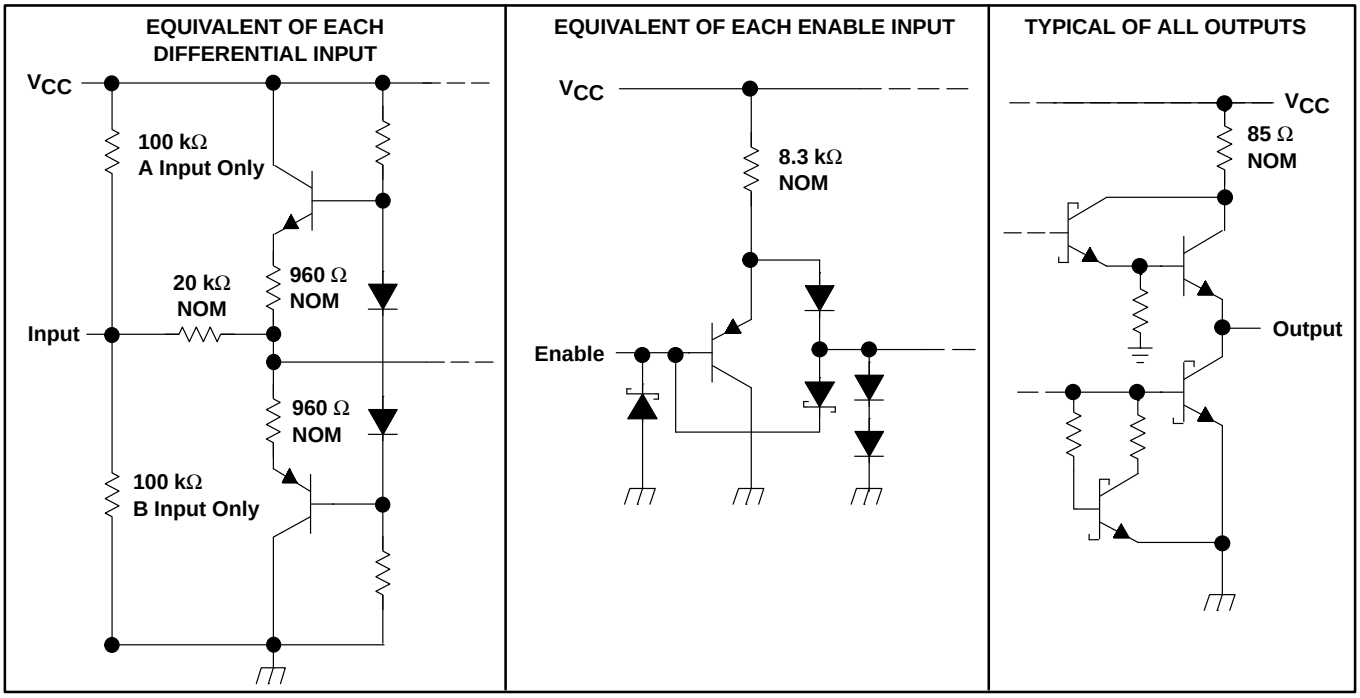


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		AM26LS32AC AM26LS33AC	AM26LS32AM AM26LS33AM	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I	Any differential input	±25	±25	V
	Other inputs	7	7	
Differential input voltage, V_{ID} (see Note 2)		±25	±25	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		0 to 70	–55 to 125	°C
Storage temperature range, T_{stg}		–65 to 150	–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Case temperature for 60 seconds, T_C	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		AM26LS32AC AM26LS33AC			AM26LS32AM AM26LS33AM			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Common-mode input voltage, V_{IC}	AM26LS32AC, AM26LS32AM			±7			±7	V
	AM26LS33AC, AM26LS33AM			±15			±15	
High-level output current, I_{OH}				–440			–440	µA
Low-level output current, I_{OL}				8			8	mA
Operating free-air temperature, T_A		0		70	–55		125	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

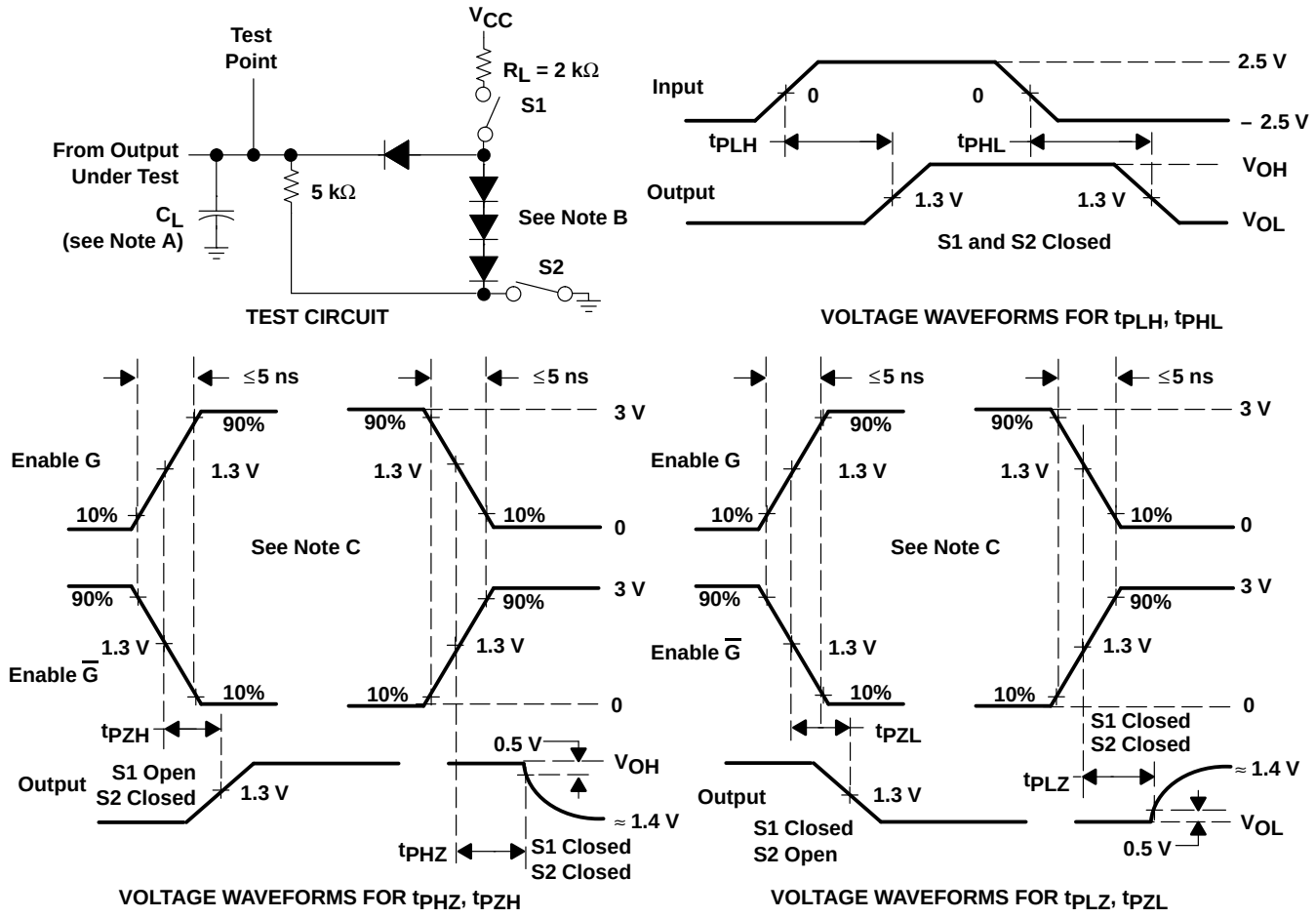
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage	$V_O = V_{OH}$min,	$I_{OH} = -440\ \mu A$	AM26LS32A			0.2	V
				AM26LS33A			0.5	
V_{IT-}	Negative-going input threshhold voltage	$V_O = 0.45$ V,	$I_{OL} = 8$ mA	AM26LS32A	−0.2‡			V
				AM26LS33A	−0.5‡			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IK}	Enable input clamp voltage	V_{CC} = MIN,	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, $V_{I(G)} = 0.8$ V,	$V_{ID} = 1$ V, $I_{OH} = -440\ \mu A$	'32AC, '33AC	2.7			V
				'32AM, '33AM	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN, $V_{I(G)} = 0.8$ V	$V_{ID} = -1$ V,	$I_{OL} = 4$ mA			0.4	V
				$I_{OL} = 8$ mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX		$V_O = 2.4$ V			20	μA
				$V_O = 0.4$ V			−20	
I_I	Line input current	$V_I = 15$ V,	Other input at −10 V to 15 V				1.2	mA
		$V_I = -15$ V,	Other input at −15 V to 10 V				−1.7	
$I_{I(EN)}$	Enable input current	$V_I = 5.5$ V					100	μA
I_{IH}	High-level enable current	$V_I = 2.7$ V					20	μA
I_{IL}	Low-level enable current	$V_I = 0.4$ V					−0.36	mA
r_I	Input resistance	$V_{IC} = -15$ V to 15 V,	One input to ac ground		12	15		kΩ
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−15		−85	mA
I_{CC}	Supply current	V_{CC} = MAX,	All outputs disabled			52	70	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$, and $V_{IC} = 0$.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15$ pF,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35	ns
t_{PZH}	Output enable time to high level	$C_L = 15$ pF,	See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level				20	25	ns
t_{PHZ}	Output disable time from high level	$C_L = 5$ pF,	See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level				30	40	ns

PARAMETER MEASUREMENT INFORMATION

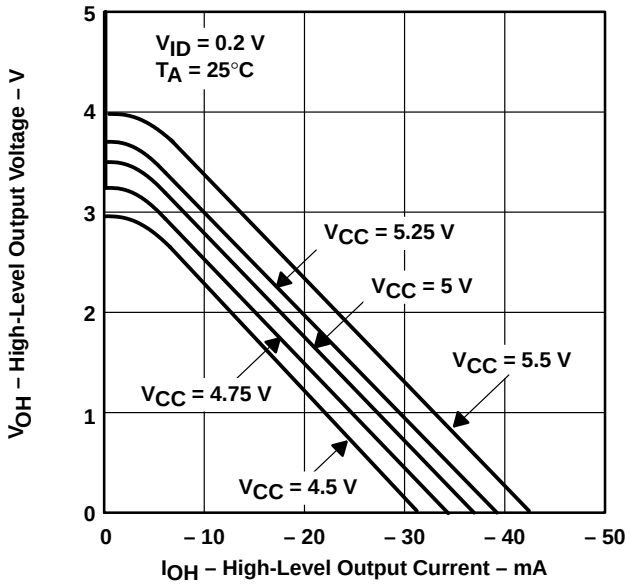


NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 1

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT†



† V_{CC} = 5.5 V and V_{CC} = 4.5 V applies to M-suffix devices only.

Figure 2

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

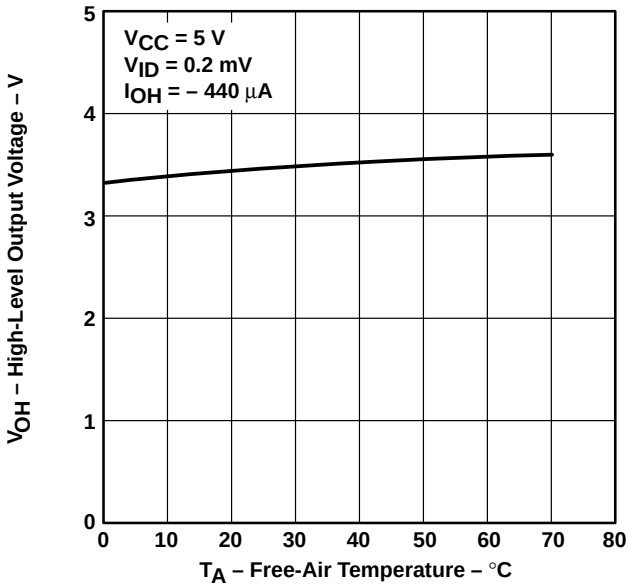


Figure 3

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

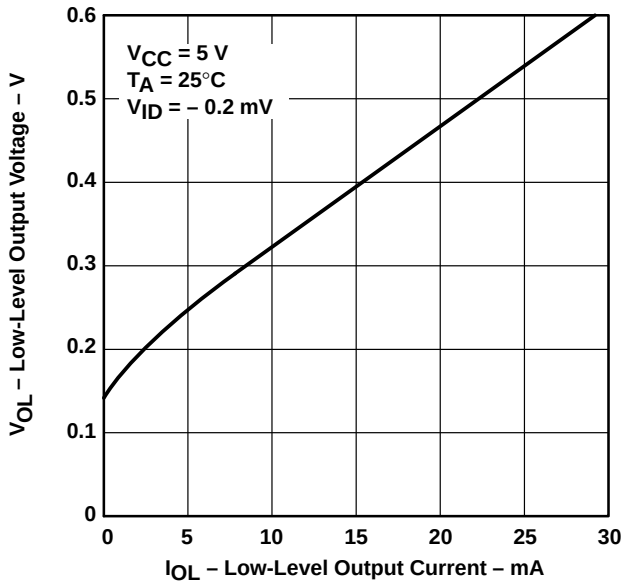


Figure 4

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

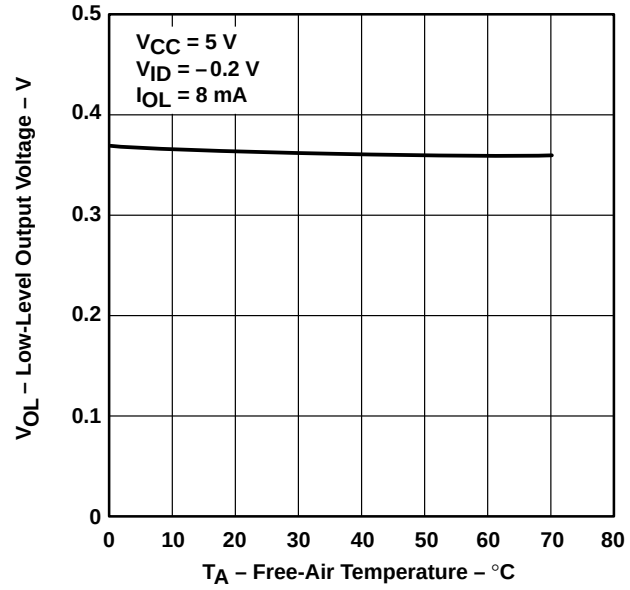


Figure 5

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

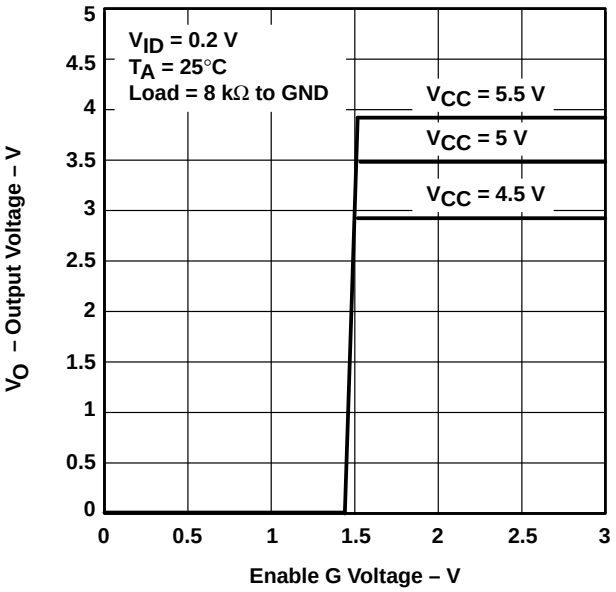


Figure 6

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

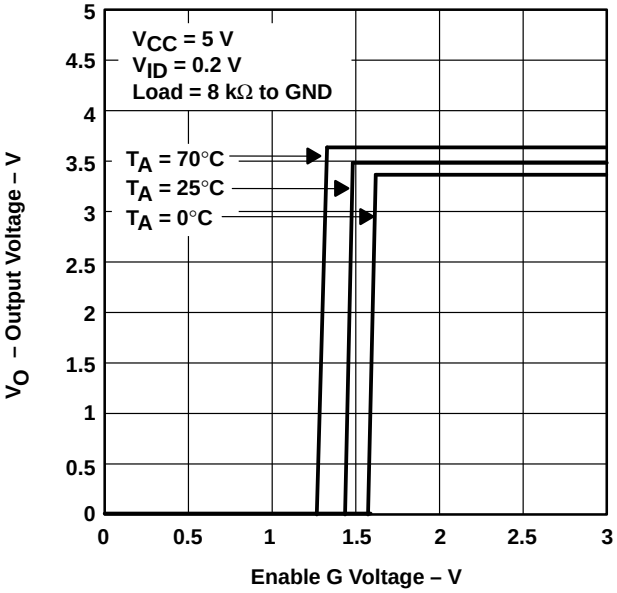


Figure 7

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

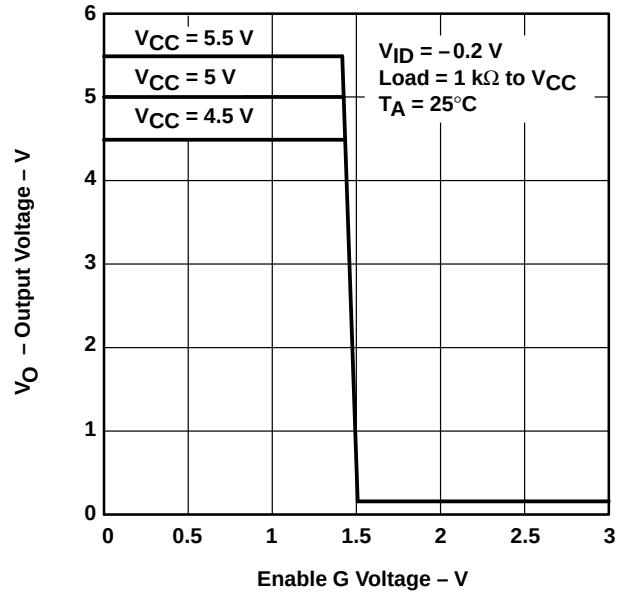


Figure 8

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

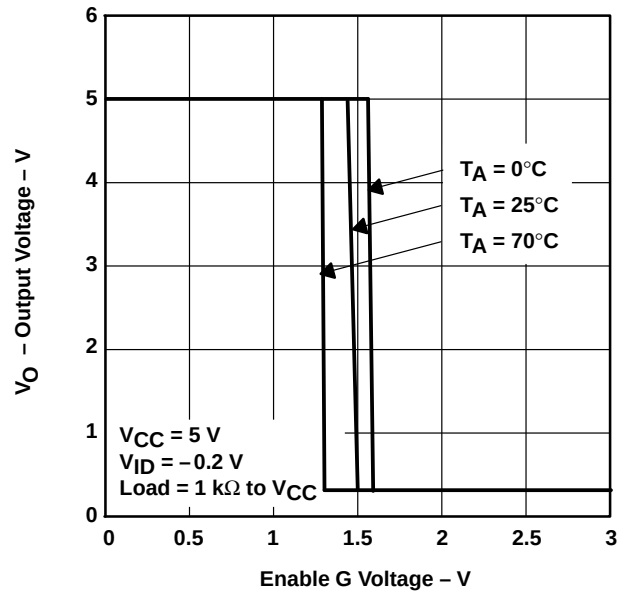


Figure 9

TYPICAL CHARACTERISTICS

AM26LS32A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

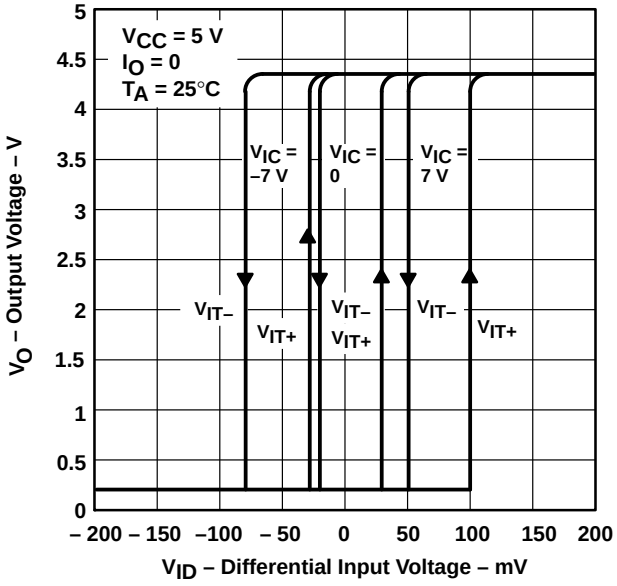


Figure 10

AM26LS33A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

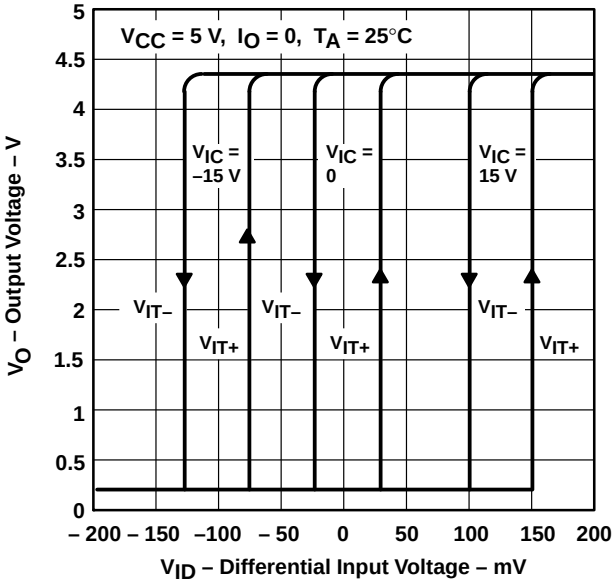
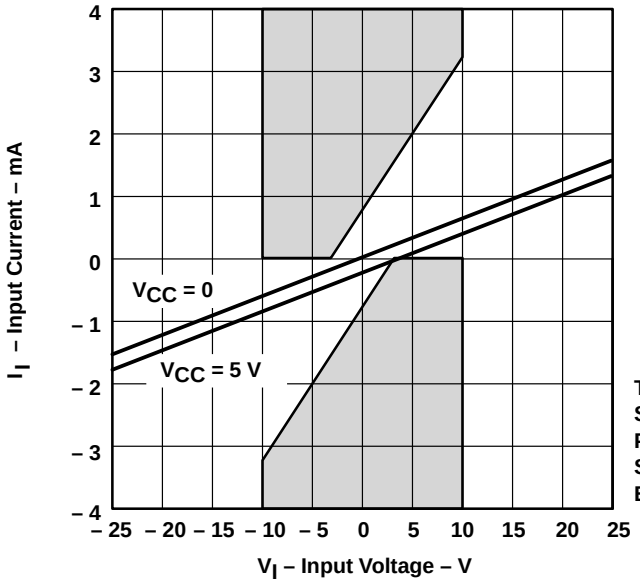


Figure 11

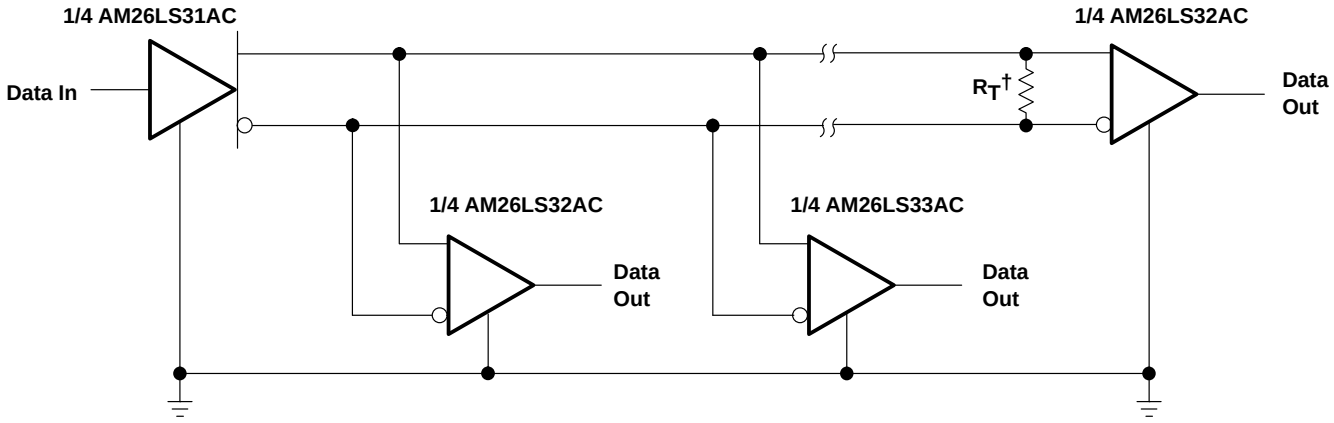
INPUT CURRENT
vs
INPUT VOLTAGE



The Unshaded Area Shows Requirements of Paragraph 4.2.1 of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B

Figure 12

APPLICATION INFORMATION



† R_T equals the characteristic impedance of the line.

Figure 13. Circuit With Multiple Receivers

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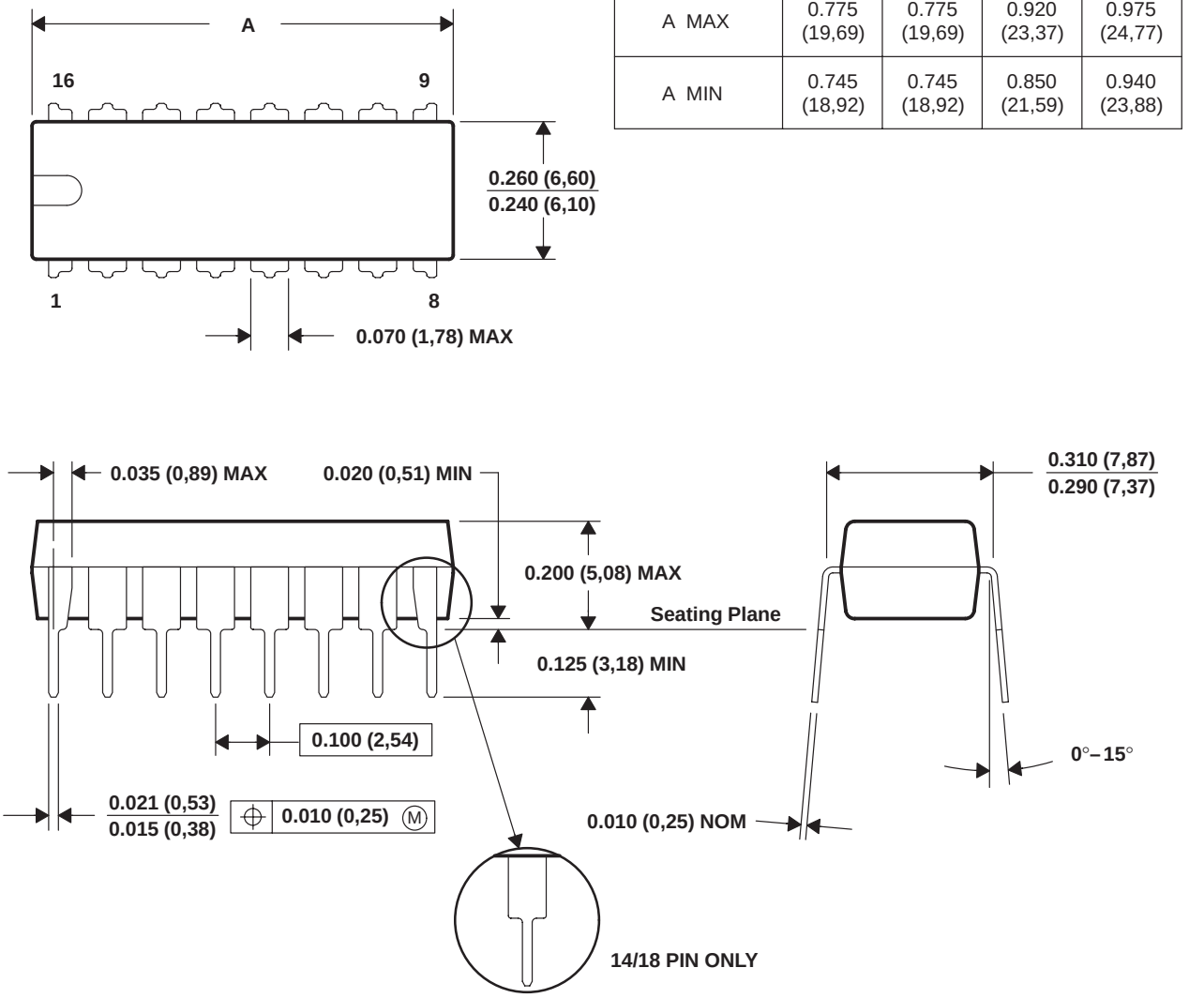
MPDI002A – JANUARY 1995 – REVISED OCTOBER 1995

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).