INTERSIL

IVN5000/1 BN Series
n-Channel Enhancement-mode
Vertical Power MOSFET

2

FEATURES

- **High speed, high peak current switching**
- **Inherent current sharing capability when paralleled**
- **Interfaces directly with CMOS, DTL, TTL logic**
- **Simple, straight-forward DC biasing**
- **Inherent protection from thermal runaway**
- **Reliable, low cost plastic package**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **High gain, broad-band VHF/UHF Amplifiers**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

These devices are Non-Zener equivalents of the VN40AF Series.

Original Type No. Zener Protected	Equiv. Type No. Non-Zener
VN40AF	IVN5001BND
VN46AF	IVN5001BND
VN66AF	IVN5001BNE
VN67AF	IVN5001BNE
VN88AF	IVN5001BNF
VN89AF	IVN5001BNF

ABSOLUTE MAXIMUM RATINGS

(25° C unless otherwise noted)

Drain-source Voltage
- IVN5000BND, IVN5001BND 40V
- IVN5000BNE, IVN5001BNE 60V
- IVN5000BNF, IVN5001BNF 80V

Drain-gate Voltage
- IVN5000BND, IVN5001BND 40V
- IVN5000BNE, IVN5001BNE 60V
- IVN5000BNF, IVN5001BNF 80V

Continuous Drain Current (see note 1) 1.7A
Peak Drain Current (see note 2) 3.0A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... -30V
Thermal Resistance, Junction to Case .... 10.4° C/W
Continuous Device Dissipation at (or below)
- 25° C Case Temperature 12W

Linear Derating Factor ..... 96mW/° C
Operating Junction
- Temperature Range ..... -40 to +150° C

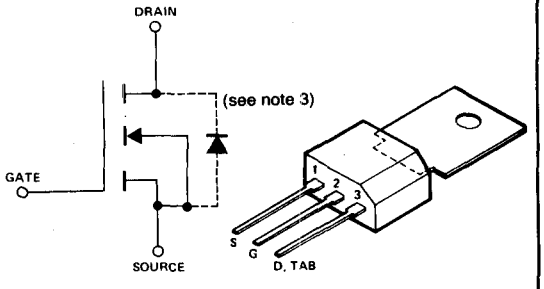
Storage Temperature Range ..... -40 to +150° C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300° C

Note 1. T_C = 25° C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

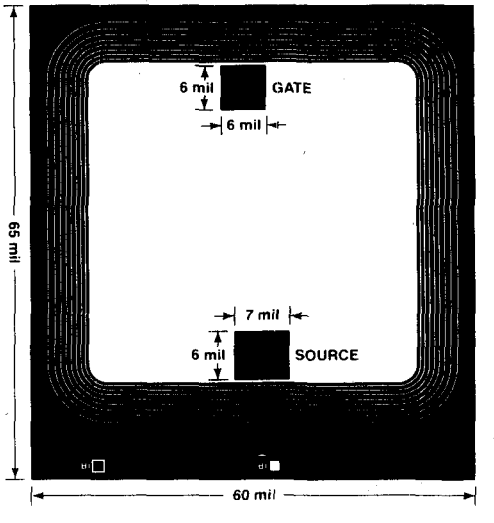
Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-202)



CHIP TOPOGRAPHY

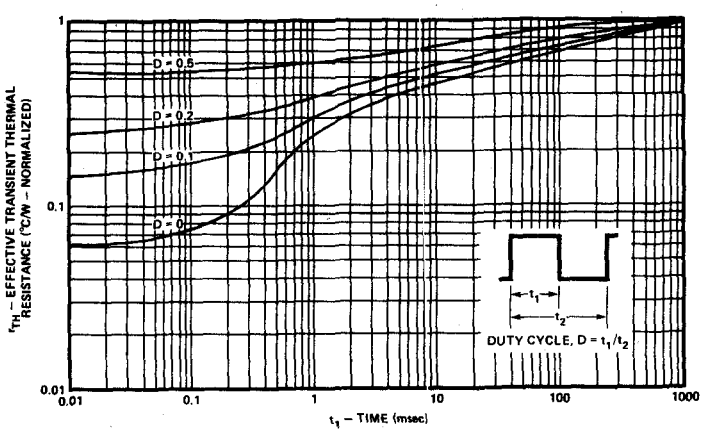


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

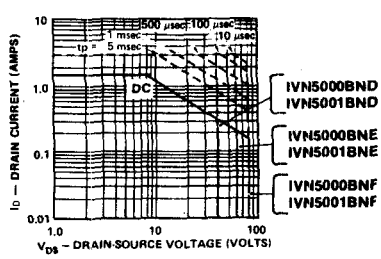
		CHARACTERISTICS		IVN5000BND IVN5001BND			IVN5000BNE IVN5001BNE			IVN5000BNF IVN5001BNF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage		40			60			80			V	V_{GS} = 0, I_D = 10μA	
2		$V_{GS(th)}$ Gate Threshold Voltage	IVN5000 Series	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
3			IVN5001 Series	0.8		3.6	0.8		3.6	0.8		3.6			
4		I_{GSS} Gate-Body Leakage			0.1	10		0.1	10		0.1	10	nA	V_{GS} = 15V, V_{DS} = 0	
5						50			50			50		V_{GS} = 15V, V_{DS} = 0, T_A = +125°C	
6		I_{DSS} Zero Gate Voltage Drain Current				10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
7						500			500			500	μA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
8					20			20			20		nA	V_{DS} = 24V, V_{GS} = 0	
9		$I_{D(on)}$ ON-State Drain Current	IVN5000 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	V_{DS} = 24V, V_{GS} = 10V	
10			IVN5001 Series	1.0	1.9		1.0	1.9		1.0	1.9			V_{DS} = 24V, V_{GS} = 12V	
11		$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5000BND IVN5000BNE IVN5000BNF		1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 0.3A	
12					2.0	2.5		2.0	2.5		2.0	2.5		V_{GS} = 10V, I_D = 1.0A	
13			IVN5001BND IVN5001BNE IVN5001BNF		1.2			1.2			1.2			V_{GS} = 7V, I_D = 0.3A	
14					1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V, I_D = 1.0A	
15		$r_{DS(on)}$ Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V, I_D = 1.0A	(Note 1)
16			IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V, I_D = 1.0A	
17	DYNAMIC	$r_{ds(on)}$ Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5		V_{GS} = 10V, I_D = 1.0A, f = 1KHz	
18			IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V, I_D = 1.0A, f = 1KHz	
19		g_{fs} Forward Transconductance		170	280		170	280		170	280		mΩ	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	
20		C_{iss} Input Capacitance			40	50		40	50		40	50	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
21		C_{oss} Output Capacitance			27	40		27	40		27	40			
22		C_{rss} Reverse Transfer Capacitance			6	10		6	10		6	10			
23		$t_{d(on)}$ Turn-ON Delay Time			2	5		2	5		2	5	ns	See Switching Times Test Circuit, page 2-42.	(Note 2)
24		t_r Rise Time			2	5		2	5		2	5			
25		$t_{d(off)}$ Turn-OFF Delay Time			2	5		2	5		2	5			
26		t_f Fall Time			2	5		2	5		2	5			

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

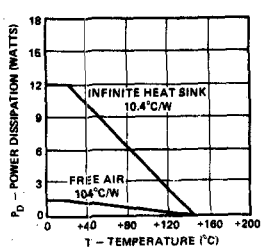
THERMAL RESPONSE



DC SAFE OPERATING REGION
T_C = 25° C



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



Note: For other 5000 family characteristic curves, see page 2-41.