STP80NF70

N-channel 68 V, 0.0082 Ω, 98 A, TO-220 STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STP80NF70	68 V	< 0.0098 Ω	98 A

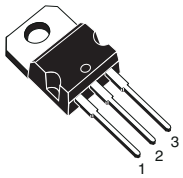
- Exceptional dv/dt capability
- 100% avalanche tested

Application

- Switching applications

Description

The STP80NF70 is a N-channel Power MOSFET realized with STMicroelectronics unique STripFET™ process. It has specifically been designed to minimize input capacitance and gate charge. The device is therefore suitable in advanced high-efficiency switching applications.



TO-220

Figure 1. Internal schematic diagram

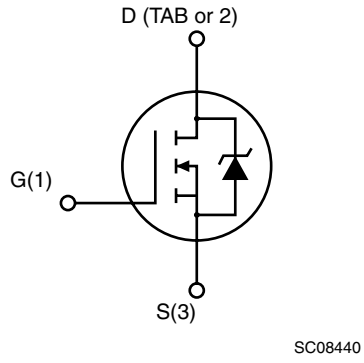


Table 1. Device summary

Order code	Marking	Package	Packaging
STP80NF70	80NF70	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	68	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	98	A
I_D	Drain current (continuous) at T_C=100 °C	68	A
I_{DM} (1)	Drain current (pulsed)	392	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	W
	Derating factor	1.27	W/°C
dv/dt (2)	Peak diode recovery voltage slope	13	V/ns
E_{AS} (3)	Single pulse avalanche energy	700	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_J	Operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 80$ A, di/dt ≤ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.
3. Starting T_J = 25 °C, I_D = 40 A, V_{DD} = 34 V.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.79	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose (1)	300	°C

1. 1.6 mm from case for 10 sec.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	68			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 40 A		0.0082	0.0098	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 40 A	-	60	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f = 1 MHz, V_{GS} = 0	-	2550 550 175	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 34 V, I_D = 80 A V_{GS} =10 V	-	75 17 30	-	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 34 V, I_D= 40 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 13 on page 9*	-	17 60 90 75	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		98	A
I_{SDM}(1)	Source-drain current (pulsed)		-		392	A
V_{SD}(2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80 A, di/dt = 100 A/µs, V_{DD} = 25 V, T_J = 150 °C *Figure 15 on page 9*	-	70 160 4.7		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

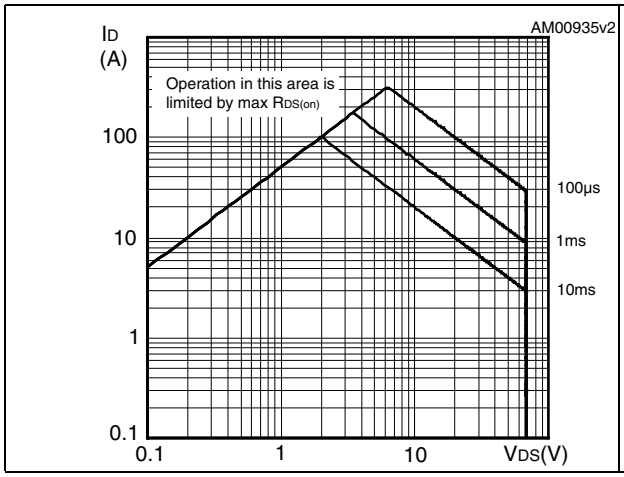


Figure 3. Thermal impedance

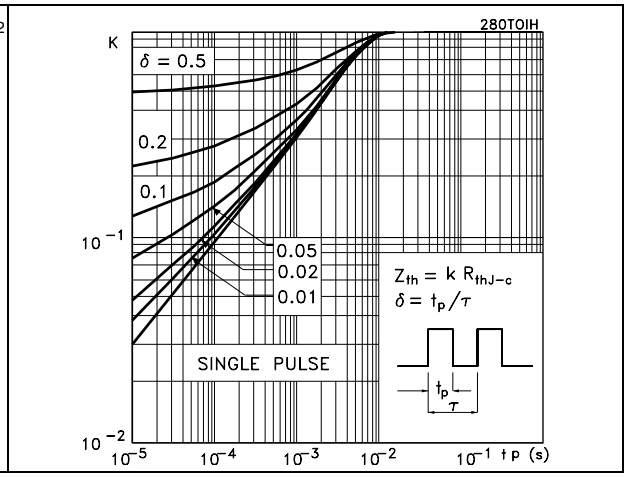


Figure 4. Output characteristics

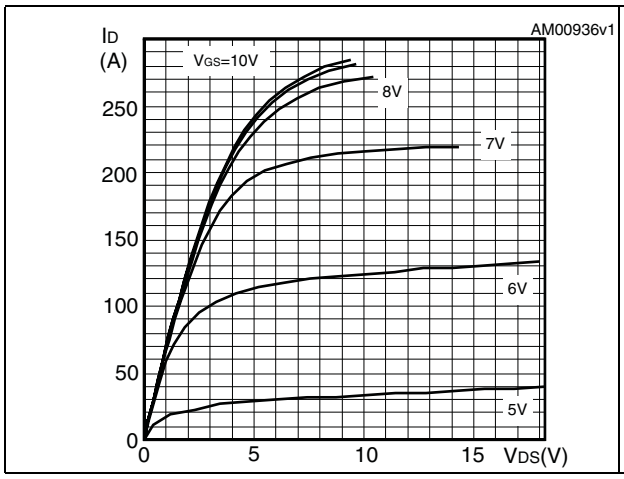


Figure 5. Transfer characteristics

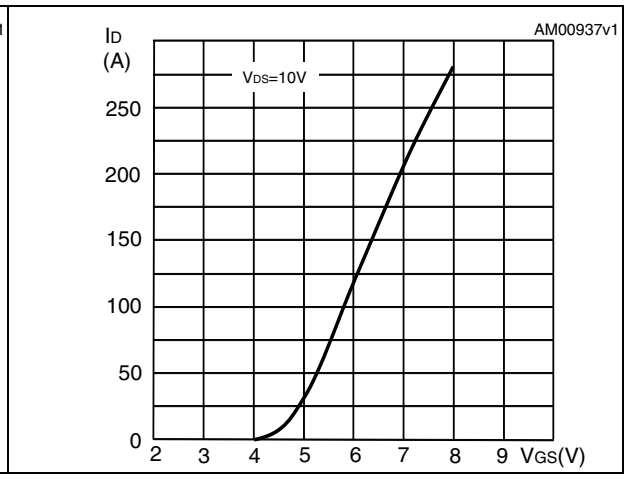


Figure 6. Normalized BV_{DSS} vs temperature

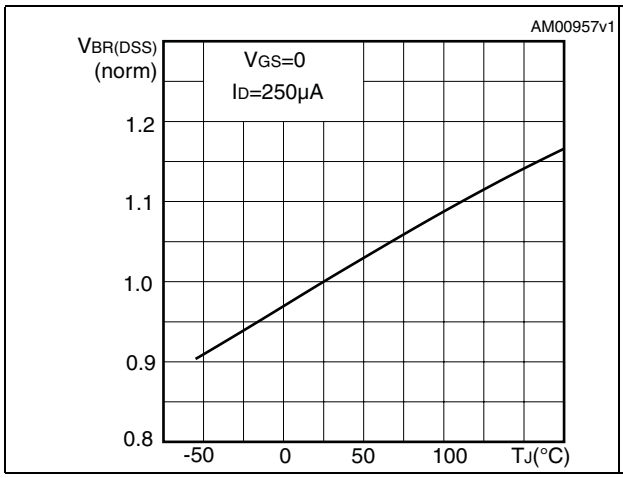


Figure 7. Static drain-source on resistance

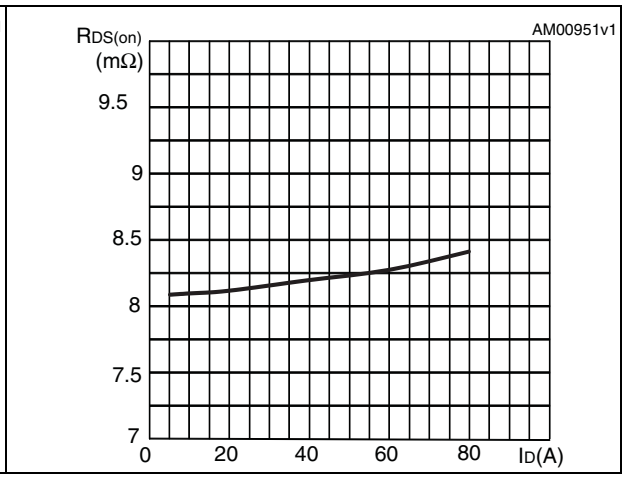


Figure 8. Gate charge vs gate-source voltage

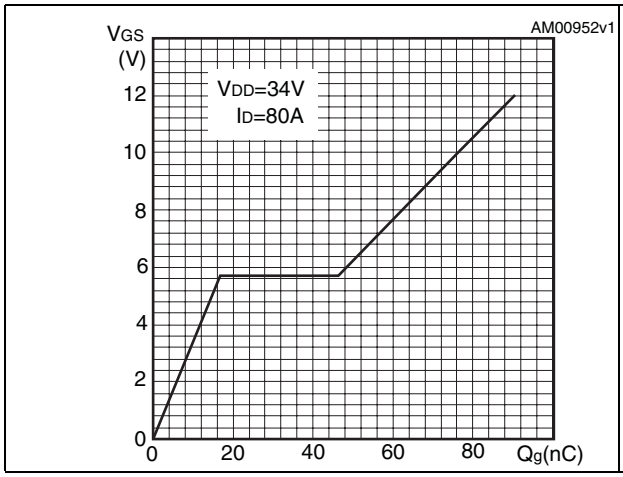


Figure 9. Capacitance variations

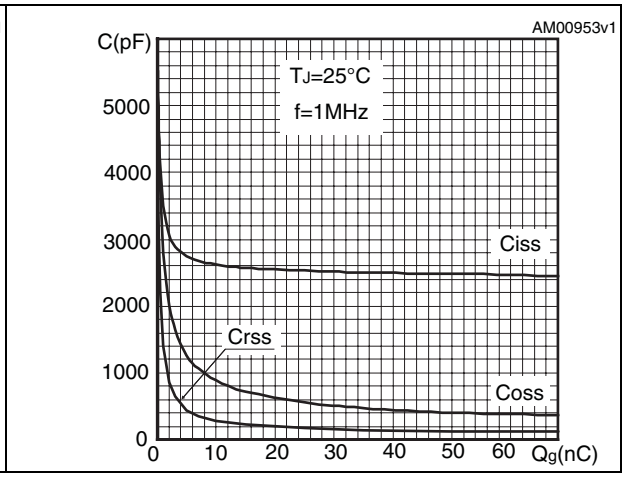


Figure 10. Normalized gate threshold voltage vs temperature

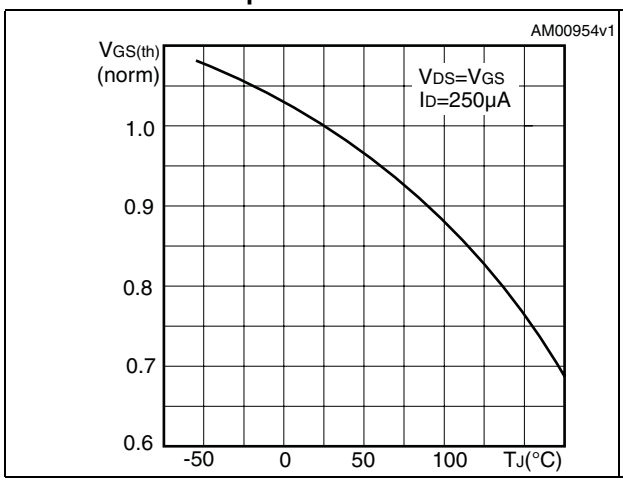


Figure 11. Normalized on resistance vs temperature

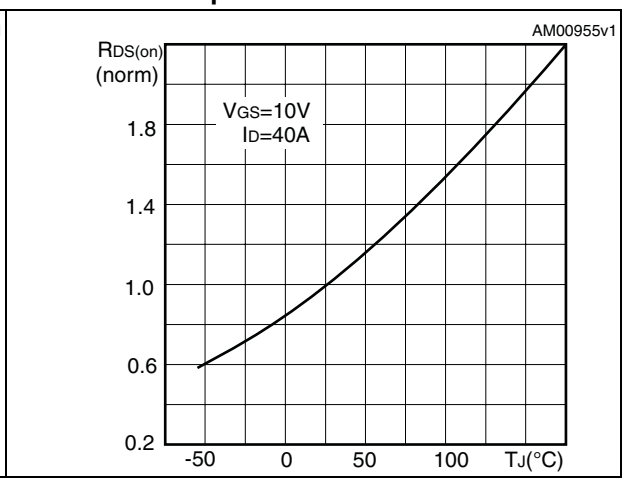
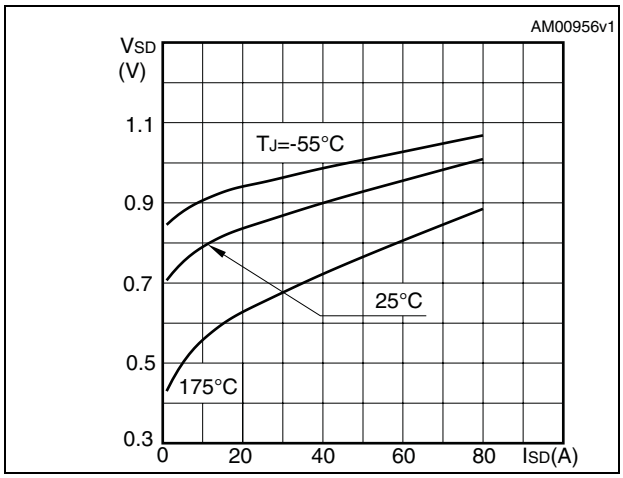


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

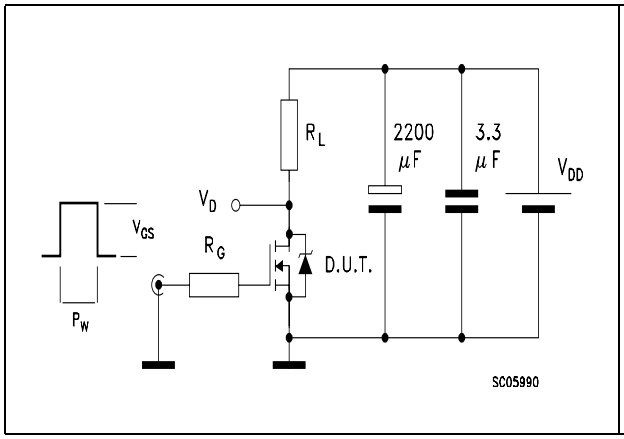


Figure 14. Gate charge test circuit

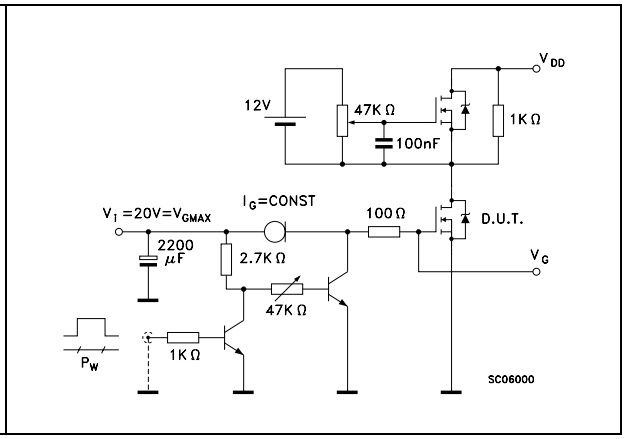


Figure 15. Test circuit for inductive load switching and diode recovery times

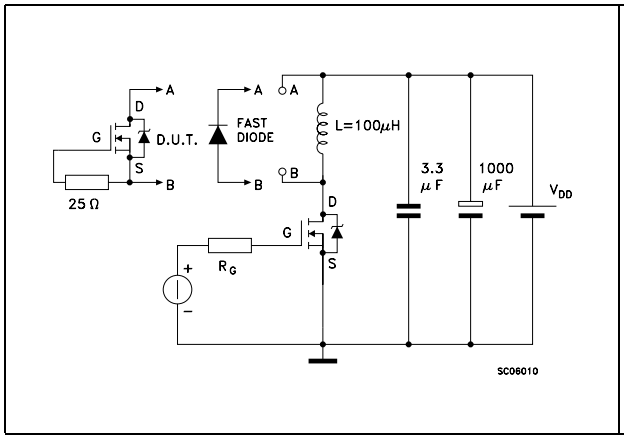


Figure 16. Unclamped inductive load test circuit

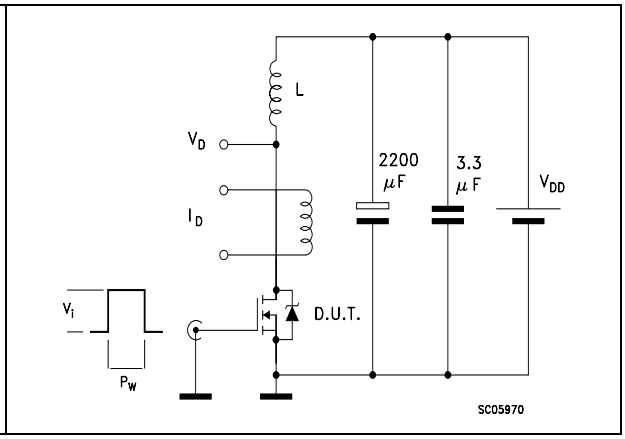
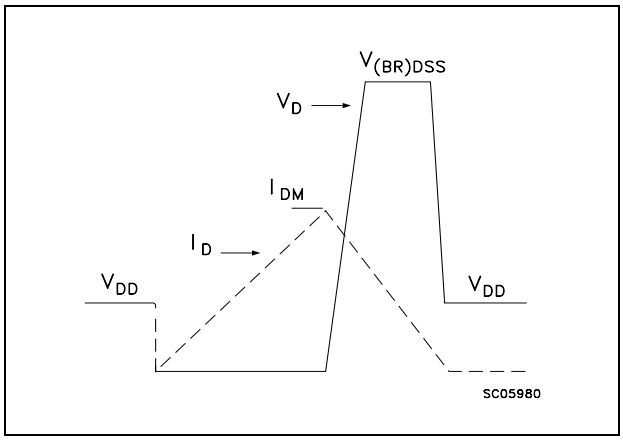


Figure 17. Unclamped inductive waveform

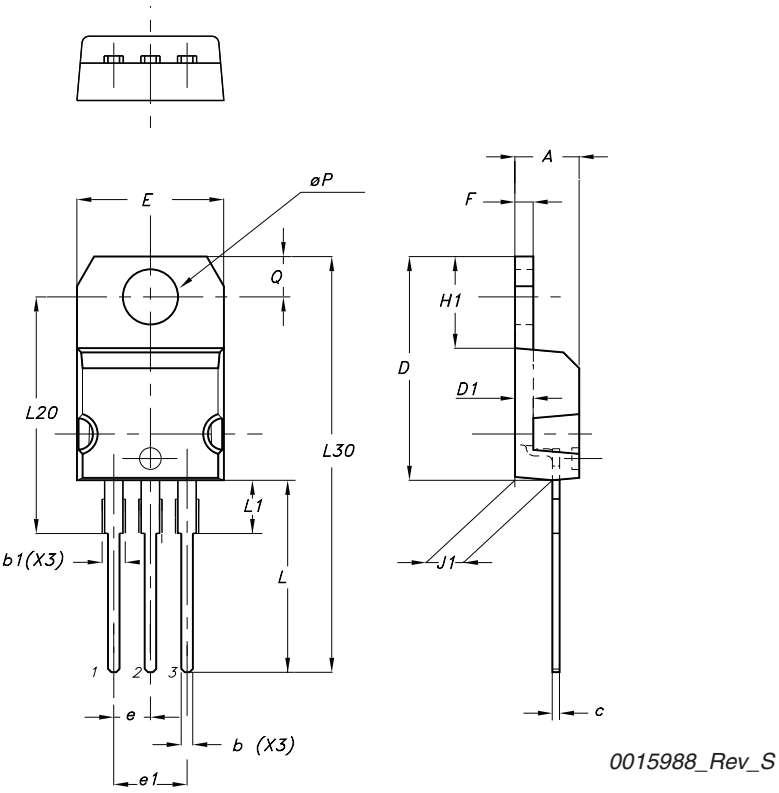


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Jun-2010	1	First release.

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