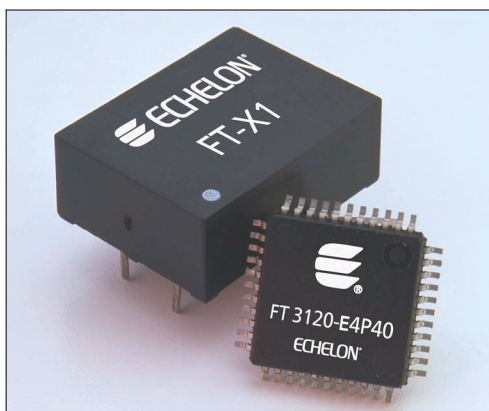


FT 3120® and FT 3150® Smart Transceivers Models 14210-500, 14220-900, and 14230-800



FT 3120 transceiver in a 44-pin TQFP package^[1]

Description

The FT 3120 and FT 3150 Smart Transceivers integrate a Neuron® 3120 or Neuron 3150 network processor core, respectively, with a free topology twisted pair transceiver to create a low cost, smart transceiver on a chip. Combined with Echelon's high performance FT-X1 Communication Transformer, the FT 3120 and FT 3150 transceivers set new benchmarks for performance, robustness, and low cost. Ideal for use in LONWORKS® nodes destined for building, industrial, transportation, home, and utility automation applications, the FT 3120 and FT 3150 Smart Transceivers can be used in both new product designs and as a means of cost reducing existing nodes.

The integral transceiver is fully compatible with the TP/FT-10 channel and can communicate with nodes using Echelon's FTT-10A Free Topology Transceiver, and, when used with suitable DC isolation capacitors, LPT-10 Link Power Transceiver. The free topology transceiver supports polarity insensitive cabling using a star, bus, daisy-chain, loop, or combination topology—freeing the installer from the need to adhere to a strict set of wiring rules. Free topology wiring reduces the time and expense of node installation by allowing the wiring to be installed in the most expeditious and cost-effective manner. It also simplifies network expansion by eliminating restrictions on wire routing, splicing, and node placement.

The FT 3120 Smart Transceiver is a complete system-on-a-chip that is targeted at cost-sensitive and small form factor designs with a need for up to 4Kbytes of application code. The Neuron 3120 core operates at up to 40MHz^[2], and includes 4Kbytes of EEPROM and 2Kbytes of RAM. The LONWORKS system firmware is pre-programmed in an on-chip ROM. The application code is stored in the embedded EEPROM memory and may be updated over the network. The FT 3120 transceiver is offered in a 32-lead SOIC package as well as a compact 44-lead TQFP package.

- ▼ Combines an ANSI/EIA 709.3-1999 compliant free topology twisted pair transceiver with a Neuron 3120 or Neuron 3150 network processor core
- ▼ Supports polarity insensitive free topology star, daisy chain, bus, loop, or mixed topology wiring
- ▼ 78 kilobits per second bit rate for distances up to 500 meters in free topology or 2700 meters in bus topology with double terminations
- ▼ High performance Neuron network processor core enables concurrent processing of application code and network packets (40MHz maximum for FT 3120 transceiver, 20MHz for FT 3150 transceiver)
- ▼ 4Kbytes of embedded EEPROM for application code and configuration data on the FT 3120 Smart Transceiver and 0.5Kbytes of embedded EEPROM for configuration data on the FT 3150 Smart Transceiver
- ▼ Interface for external memory for nodes with larger memory requirements (FT 3150 Smart Transceiver only)
- ▼ 2Kbytes of embedded RAM for buffering network data and network variables
- ▼ 11 I/O pins with 34 programmable standard I/O modes minimizing external interface circuitry
- ▼ Unique 48-bit ID in every device for network installation and management
- ▼ Compact external transformer with patent pending architecture providing exceptional immunity from magnetic interference and high frequency common mode noise
- ▼ Compatible with TP/FT-10 channels using FTT-10 and/or FTT-10A Free Topology Transceivers and, with suitable DC blocking capacitors, LPT-10 Link Power Transceivers
- ▼ 5V operation with low power consumption
- ▼ -40 to +85°C operating temperature range^[3]

The FT 3150 Smart Transceiver includes a 20MHz Neuron 3150 core, 0.5Kbytes of EEPROM and 2Kbytes of RAM. Through its external memory bus, the FT 3150 transceiver can address up to 58Kbytes of external memory, of which 16Kbytes of external non-volatile memory is dedicated to the LONWORKS system firmware. The FT 3150 transceiver is supplied in a 64-lead TQFP package.

The embedded EEPROM may be written up to 10,000 times with no data loss. Data stored in the EEPROM will be retained for at least 10 years.^[3]

Three different versions of the FT 3120 and FT 3150 Smart Transceivers are available to meet a wide range of applications and packaging requirements. See the table on FT 3120 and FT 3150 Smart Transceiver Ordering Information for product offerings and descriptions.

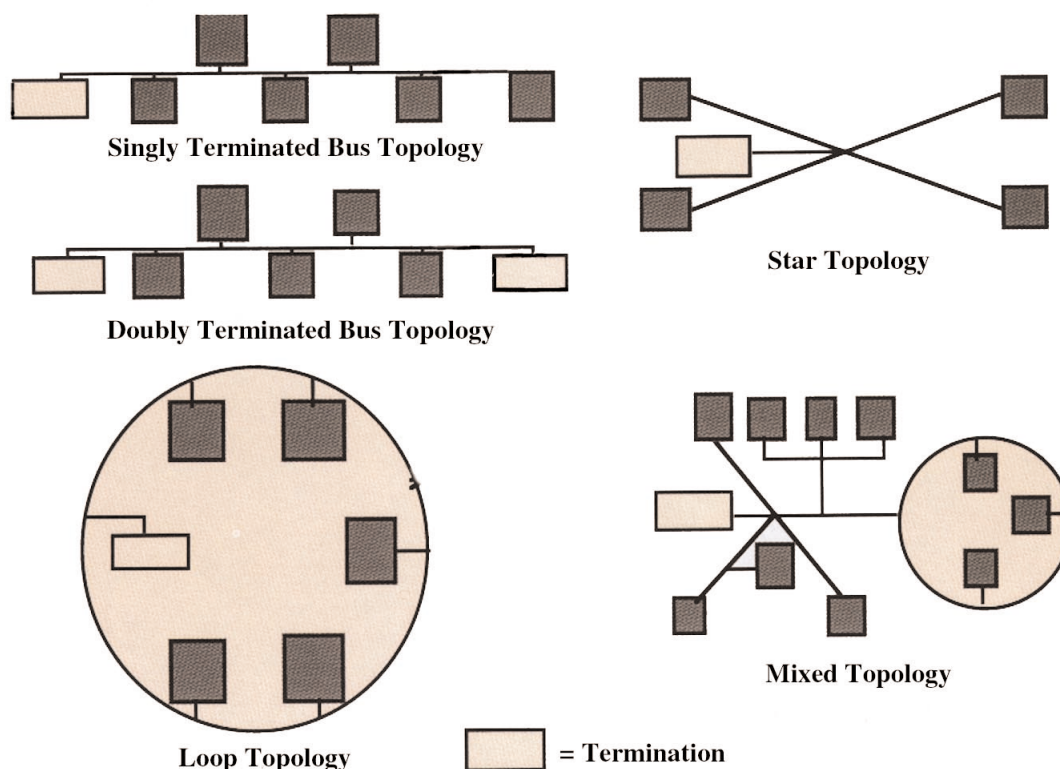
Notes:

¹ See table on FT 3120 and FT 3150 Smart Transceiver Ordering Information for other product offerings and description.

² The FT 3120 Smart Transceiver is designed to run at frequencies up to 40MHz using an external clock oscillator. It is important to note that external oscillators may typically take on the order of 5ms to stabilize after power-up. The Neuron Chip should be held in reset until the CLK1 input is stable. With some oscillators, this may require the use of a reset stretching Low-Voltage Detection chip/circuit. Check the oscillator specifications for more information on startup stabilization times.

³ EEPROM Programming must be limited to -25 to 85°C for a guaranteed 10-year data retention over the -40 to 85°C operating temperature range.

Typical Free Topologies Supported by the FT 3120 and FT 3150 Smart Transceivers



Flexible I/O, Simple Configuration

The FT 3120 and FT 3150 Smart Transceivers provide 11 I/O pins which may be configured to operate in one or more of 34 predefined standard input/output modes. Combining a wide range of I/O models with two on-board timer/counters enable the FT 3120 and FT 3150 transceivers to interface to application circuits with minimal external logic or software development.

Easy Interface to Any Host MCU

The FT 3120 and FT 3150 Smart Transceivers can be easily interfaced to other host MCUs via Echelon's ShortStack™ or MIP firmware. When used with the ShortStack or MIP firmware, the Smart Transceiver enables any OEM product with a host microcontroller to quickly and inexpensively become a networked, Internet-accessible device. The ShortStack firmware uses an SCI or SPI serial interface to communicate between the host and the Smart Transceiver. The MIP uses a high performance parallel or dual-ported RAM interface.

Advanced Network Noise Protection

The FT 3120 and FT 3150 transceivers are supplied with a patent pending external communication transformer. This transformer enables operation in the presence of high frequency common mode noise on unshielded twisted pair networks. Properly designed nodes can meet the rigorous Level 3 requirements of EN 61000-4-6 without the need for a network isolation choke.

The transformer also offers outstanding immunity from magnetic noise, eliminating the need for protective magnetic shields in most applications. The transformer is provided in a potted, 6-pin, through-hole plastic package.

The FT-X1 Communication Transformer must be ordered separately. See the table on FT 3120 and FT 3150 Smart Transceiver Ordering Information for product offerings and descriptions. Both the FT 3120 / FT 3150 Smart Transceiver IC and the FT-X1 Communication Transformer are designed to be used as a pair and therefore must be implemented together in all designs. If a transformer other than the FT-X1 Communication Transformer is used with either the FT 3120 or FT 3150 Smart Transceiver IC, then Echelon cannot guarantee the performance of the FT 3120 or FT 3150 Smart Transceiver and in that event, the warranty for the FT 3120 or FT 3150 Smart Transceiver will be void.

A typical FT 3120 or FT 3150-based node requires a power source, crystal and an I/O interface to the device being controlled (see figure for a typical FT 3120 / FT 3150-based node).

Preserve Your Software and Hardware Investment While Upgrading

The FT 3120 Smart Transceiver is pin compatible with Neuron 3120 Chips from Motorola and Toshiba while the FT 3150 Smart Transceiver is pin compatible with Neuron 3150 Chips from Motorola and Toshiba. The 6-pin through-hole communication transformer is pin compatible with Echelon's 9-pin FTT-10A Twisted Pair Transceiver and is keyed to prevent accidental reversal during insertion in the printed circuit card. In most cases the FT 3120 and FT 3150 IC will directly replace a Neuron Chip, and the FT-X1 Communication Transformer will replace the FTT-10A Transceiver in an existing design without requiring any layout changes, only a recompilation of the application code.^[4]

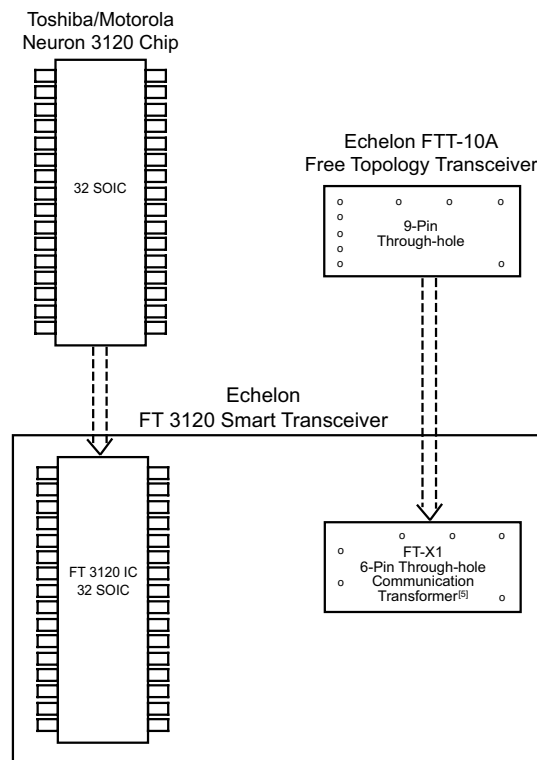
The figure below presents a block diagram view of how an FT 3120-E4S40 IC and FT-X1 Communication Transformer will replace a 32-pin SOIC Neuron 3120 Chip and FTT-10A Transceiver.

Software Updates necessary to support the Smart Transceivers on Echelon's LonBuilder® and NodeBuilder® development tools are available from Echelon's Web site at www.echelon.com. Programming solutions for the FT 3120 Smart Transceiver are available from BP Microsystems, Hi/Lo, and System General from their portfolio of universal device programmers. The FT 3120 Smart Transceiver is also compatible with the previous generation Model 21700 Neuron 3120 Chip Programmer from Echelon.

End-to-End Solutions

Echelon provides all of the building blocks required to successfully design and field cost-effective, robust products based on the FT 3120 and FT 3150 Smart Transceivers. Our end-to-end solutions include a comprehensive set of development tools, network interfaces, routers, and network management tools. Pre-production design review services, training, and worldwide technical support—including on-site support—are available through Echelon's LonSupport™ technical assistance program.

Upgrading to an FT 3120-E4S40 IC and FT-X1 Communication Transformer from a 32-pin SOIC Neuron 3120 Chip and FTT-10A

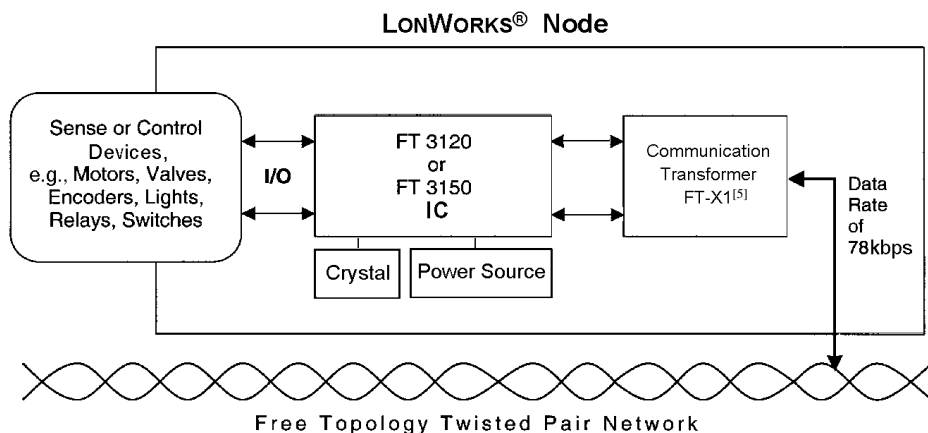


Notes:

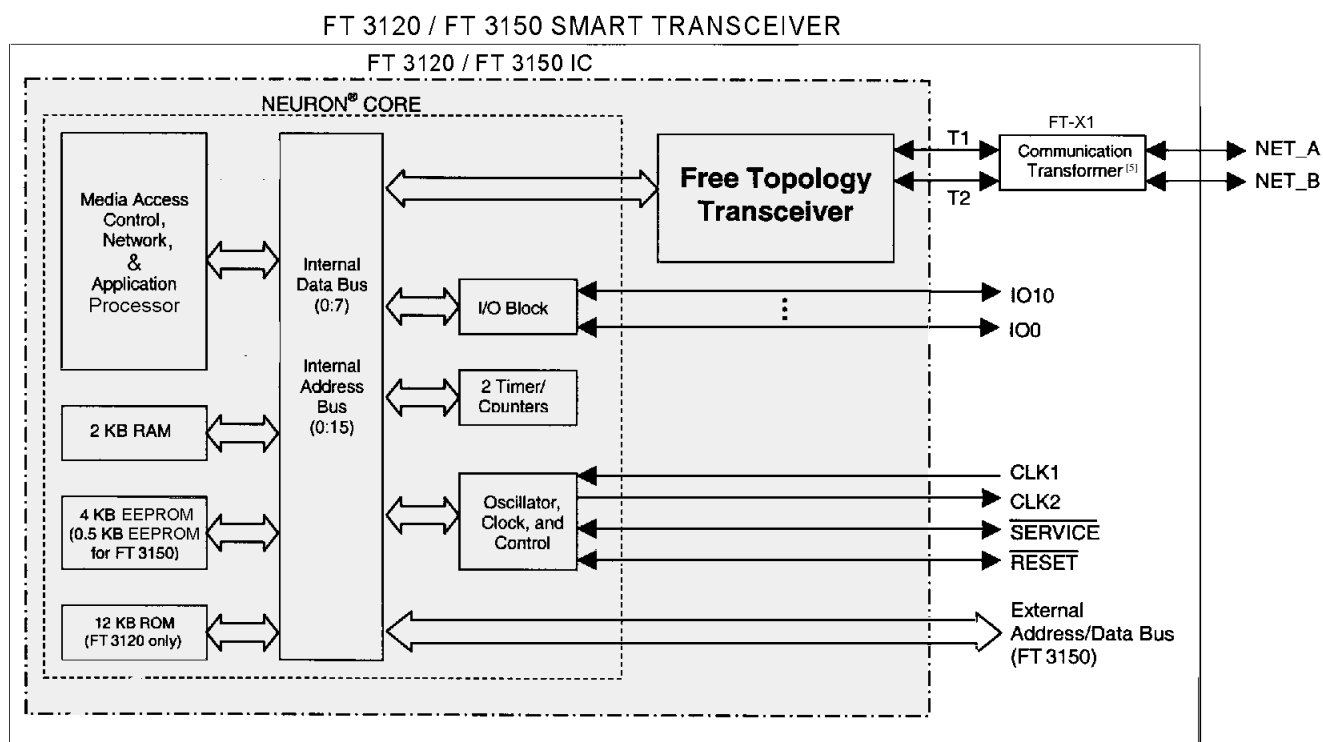
⁴ Certain nodes providing Rx packet detection LEDs may not be pin compatible with the FT 3120 and FT 3150 Smart Transceiver. Contact Echelon for details.

⁵ The FT-X1 Communication Transformer must be ordered separately and must be used with the FT 3120 / FT 3150 Smart Transceiver IC in all designs.

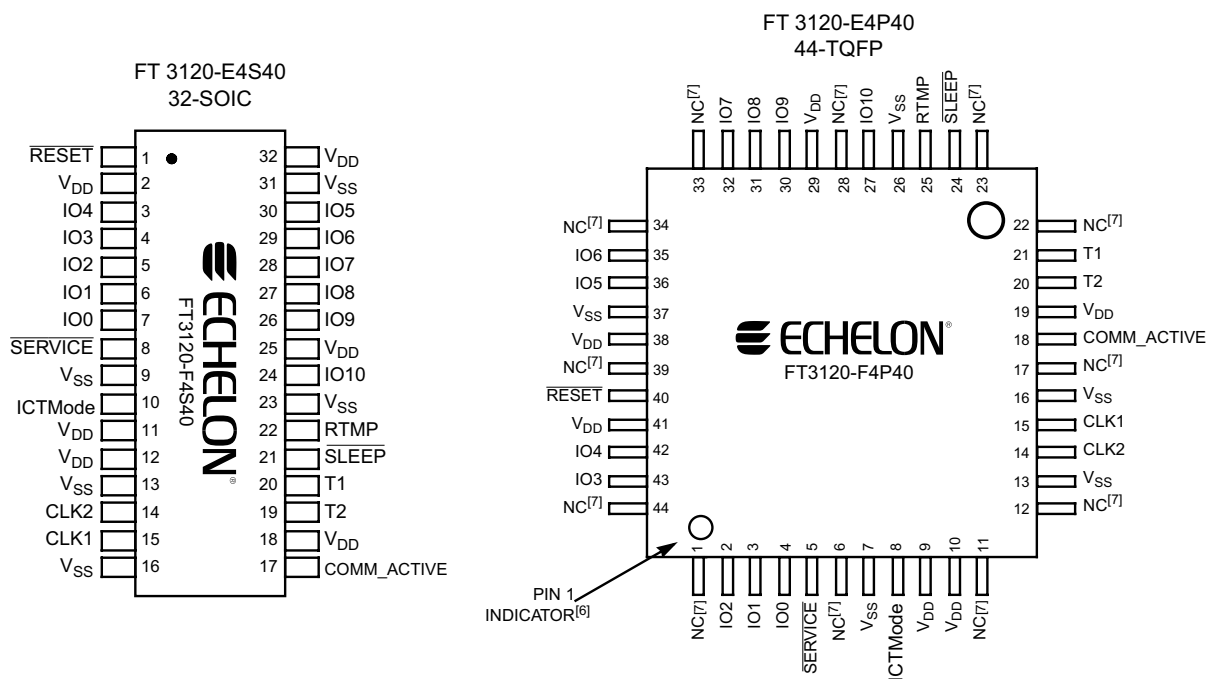
Typical FT 3120 / FT 3150 Smart Transceiver-based Node



FT 3120 / FT 3150 Smart Transceiver Block Diagram



FT 3120 / FT 3150 Smart Transceiver IC Pin Configurations



Notes:

⁵ The smaller dimple at the bottom left of the marking indicates pin 1.

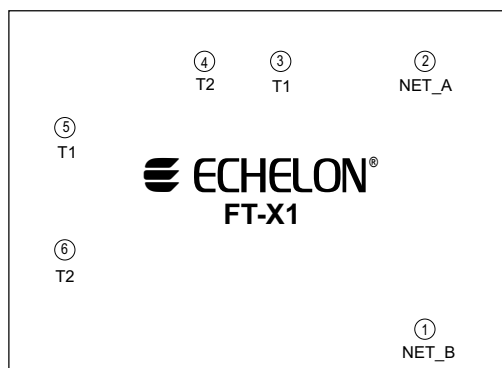
⁶ NC (No Connect) — Should not be used. (These pins are reserved for internal testing.)

FT 3120 / FT 3150 Smart Transceiver IC Pin Descriptions

Pin Name	Type	Pin Functions	FT 3150-P20 TQFP-64 Pin Number	FT 3120-E4S40 SOIC-32 Pin Number	FT 3120-E4P40 TQFP-44 Pin Number
CLK1	Input	Oscillator connection or external clock input.	24	15	15
CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1. One load.	23	14	14
$\overline{\text{RESET}}$	I/O (Built-in Pull-up)	Reset pin (active LOW). Note: The allowable external capacitance connected to the $\overline{\text{RESET}}$ pin is 100pF-1000pF.	6	1	40
$\overline{\text{SERVICE}}$	I/O (Built-in Configurable Pull-up)	Service pin (active LOW). Alternates between input and output at a 76Hz rate.	17	8	5
IO0-IO3	I/O	Large current-sink capacity (20mA). General I/O port. The output of timer/counter 1 may be routed to IO0. The output of timer/counter 2 may be routed to IO1.	2, 3, 4, 5	7, 6, 5, 4	4, 3, 2, 43
IO4-IO7	I/O (Built-in Configurable Pull-up)	General I/O port. The input of timer/counter 1 may be derived from one of IO4-IO7. The input to timer/counter 2 may be derived from IO4.	10, 11, 12, 13	3, 30, 29, 28	42, 36, 35, 32
IO8-IO10	I/O	General I/O port. May be used for serial communication under firmware control.	14, 15, 16	27, 26, 24	31, 30, 27
D0-D7	I/O	Bi-directional memory data bus.	43, 42, 38, 37, 36, 35, 34, 33	N/A	N/A
$\overline{\text{R}}/\overline{\text{W}}$	Output	Read/write control output for external memory.	45	N/A	N/A
$\overline{\text{E}}$	Output	Enable clock control output for external memory.	46	N/A	N/A
A0-A15	Output	Memory address output port.	47, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60 61, 62, 63, 64	N/A	N/A
V _{DD}	Power	Power input (5 V nom). All V _{DD} pins must be connected together externally.	7, 20, 22, 26, 40, 41, 44	2, 11, 12, 18, 25, 32	9, 10, 19, 29, 38, 41
V _{SS}	Power	Power input (0 V, GND). All V _{SS} pins must be connected together externally.	8, 19, 21, 25, 39	9, 13, 16, 23, 31	7, 13, 16, 26, 37
ICTMode	Input	In-circuit test mode control. Driving the ICTMode high and $\overline{\text{RESET}}$ low will put the device in the In-Circuit Test mode (all pins are placed in a high impedance state).	9	10	8
T1	I/O	Analog pin to be interfaced with T1 of the external transformer. Corresponds to CP0 on Toshiba, Motorola, and Cypress Neuron Chips.	28	19	20
T2	I/O	Analog pin to be interfaced with T2 of the external transformer. Corresponds to CP1 on Toshiba, Motorola, and Cypress Neuron Chips.	29	20	21
COMM_ACTIVE	Output	May be used to monitor, transmit/receive activity. Driven high during data transmissions, driven low when receiving data and kept at high impedance otherwise.	30	17	18
SLEEP	Output	SLEEP. May be configured as an output to indicate when the FT 3120 / FT 3150 is in sleep mode. Corresponds to CP3 on Toshiba, Motorola, and Cypress Neuron Chips.	31	21	24
RTMP	Input	Reserved for future use. Must be pulled up to 5V. Corresponds to CP4 on Toshiba, Motorola, and Cypress Neuron Chips.	32	22	25
NC	—	No connect. Must be left open.	1, 18, 27, 48, 49	N/A	1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44

FT-X1 Communication Transformer^[5] Pin Configuration

6-pin through-hole transformer (top view)



FT-X1 Communication Transformer Pin Descriptions

Pin Name	Pin Function	Transformer Pin Number
NET_A	Network port, polarity insensitive	2
NET_B	Network port, polarity insensitive	1
T1	Connects to the T1 pin on the FT 3120 / FT 3150 IC. Internally connected to pin 5. Corresponds to the RXD pin on the FTT-10A.	3
T2	Connects to the T2 pin on the FT 3120 / FT 3150 IC. Internally connected to pin 6. Corresponds to the TXD pin on the FTT-10A.	4
T1	Connects to the ESD/transient protection circuitry. Internally connected to pin 3. Corresponds to the T1 pin on the FTT-10A.	5
T2	Connects to the ESD/transient protection circuitry. Internally connected to pin 4. Corresponds to the T2 pin on the FTT-10A.	6

Electrical Characteristics (V_{DD} = 4.75-5.25V)

Parameter	Description	Min.	Typ.	Max.	Unit
V _{IL}	Input Low Voltage IO0-IO10, SERVICE, D0-D7, RESET			0.8	V
V _{IH}	Input High Voltage IO0-IO10, SERVICE, D0-D7, RESET	2.0			V
V _{OL}	Low-Level Output Voltage I _{out} < 20μA Standard Outputs (I _{OL} = 1.4 mA) ^[8] High Sink (IO0-IO3), SERVICE, RESET (I _{OL} = 20 mA) High Sink (IO0-IO3), SERVICE, RESET (I _{OL} = 10 mA) Maximum Sink (COMM_ACTIVE) (I _{OL} = 40 mA) Maximum Sink (COMM_ACTIVE) (I _{OL} = 15 mA)			0.1 0.4 0.8 0.4 1.0 0.4	
V _{OH}	High-Level Output Voltage I _{out} < 20μA Standard Outputs (I _{OH} = -1.4 mA) ^[8] High Sink (IO0-IO3), SERVICE (I _{OH} = -1.4 mA)	V _{DD} - 0.1 V _{DD} - 0.4 V _{DD} - 0.4			V
V _{hys}	Hysteresis (Excluding CLK1)	175			mV
I _{in}	Input Current (Excluding Pull-ups) (V _{SS} to V _{DD}) ^[9]			+/- 10	μA
I _{pu}	Pull-up Source Current (V _{out} = 0 V, Output = High-Z) ^[9]	60		260	μA
I _{DD}	Operating Mode Supply Current ^[10, 11, 12] 40MHz Clock	I _{DD} (receive) I _{DD} (transmit)	— —	68 83	mA mA
	20MHz Clock	I _{DD} (receive) I _{DD} (transmit)	— —	42 57	mA mA
	10MHz Clock	I _{DD} (receive) I _{DD} (transmit)	— —	35 50	mA mA
	5MHz Clock	I _{DD} (receive) I _{DD} (transmit)	— —	20 35	mA mA

LVI Trip Point (V_{DD})

Part Number	Min.	Typ.	Max.	Unit
FT 3120 and FT 3150	3.8	4.1	4.4	V

External Memory Interface Timing — FT 3150 (V_{DD} = 4.75 to 5.25 V, T_A = -40 to +85 C)^[3]

Parameter	Description	Min.	Max.	Unit
t _{cyc}	Memory Cycle Time (System Clock Period) ^[12]	100	3200	ns
PW _{EH}	Pulse Width, $\bar{E}$ High ^[13]	t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
PW _{EL}	Pulse Width, $\bar{E}$ Low	t _{cyc} /2 - 5	t _{cyc} /2 + 5	ns
t _{AD}	Delay, $\bar{E}$ High to Address Valid ^[17]		30	ns
t _{AH}	Address Hold Time After $\bar{E}$ High ^[17]	9		ns
t _{RD}	Delay, $\bar{E}$ High to R/W Valid Read ^[17]		14	ns
t _{RH}	R/W Hold Time Read After $\bar{E}$ High	5		ns
t _{WR}	Delay, $\bar{E}$ High to R/W Valid Write		14	ns
t _{WH}	R/W Hold Time Write After $\bar{E}$ High	5		ns
t _{DSR}	Read Data Setup Time to $\bar{E}$ High	15		ns
t _{DHR}	Data Hold Time Read After $\bar{E}$ High	0		ns
t _{DHW}	Data Hold Time Write After $\bar{E}$ High ^[14, 15]	10		ns
t _{DDW}	Delay, $\bar{E}$ Low to Data Valid		12	ns
t _{DHZ}	Data Tri-State Hold Time After $\bar{E}$ Low ^[16]	6		ns
t _{DDZ}	Delay, $\bar{E}$ High to Data Three-State ^[16]		42	ns
t _{acc}	External Memory Access Time (t _{acc} = t _{cyc} - t _{AD} - t _{DSR}) at 20MHz Input Clock		55 ^[18]	ns

Notes:

⁸ Standard outputs are IO4-IO10. (RESET is an open drain input/output. CLK2 must have ≤ 15pF load.) For FT 3150, standard outputs also include A0-A15, D0-D7, $\bar{E}$, and R/W.

⁹ IO4-IO7 and SERVICE have configurable pull-ups. RESET has a permanent pull-up.

¹⁰ Supply current measurement conditions: all outputs under no-load conditions, all inputs ≤ 0.2V or ≥ (V_{DD} - 0.2V), configurable pull-ups off and crystal oscillator clock input disabled.

¹¹ Typical values are at midpoint of supply voltage range and 25°C only.

¹² Typical IDD for 40MHz operation is 53mA. For operation above 70°C, care must be taken to not raise the device junction temperature above 100°C.

¹³ t_{cyc} = 2/f where f is the input clock (CLK1) frequency (20, 10, 5, 2.5, 1.25, or 0.625 MHz)

¹⁴ Refer to Figure 3 for detailed measurement information.

¹⁵ The data hold parameter, t_{DHW}, is measured to disable levels shown in Figure 7, rather than to the traditional data invalid levels.

¹⁶ Refer to Figure 6 and Figure 7 for detailed measurement information.

¹⁷ The three-state condition is when the device is not actively driving data. Refer to Figure 2 and Figure 5 for detailed measurement information.

¹⁸ To meet the timing above for 20MHz operation, the loading on A0-A15, D0-D7, and R/W is 30pF. Loading on $\bar{E}$ is 20pF.

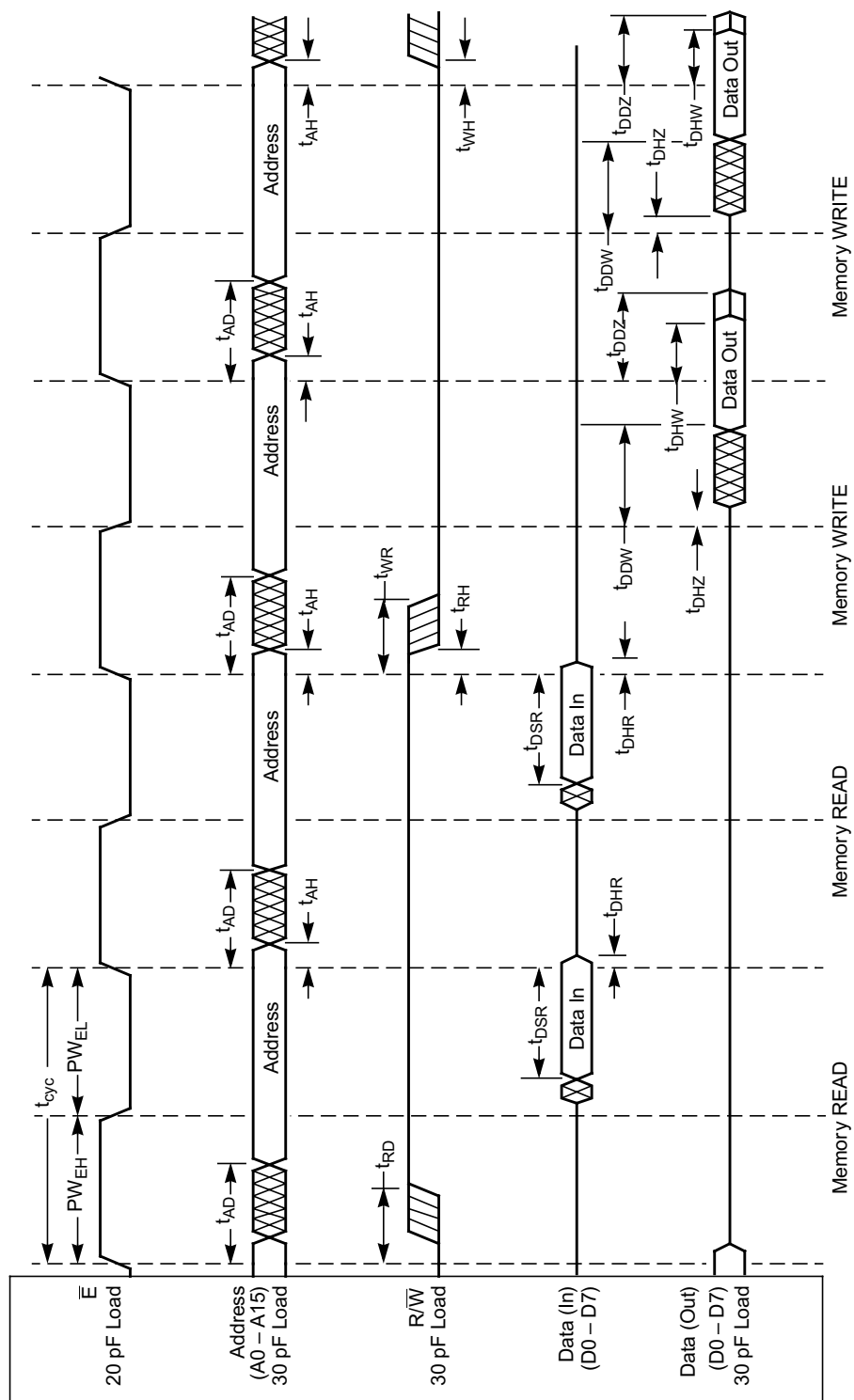
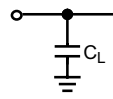


Figure 1. External Memory Interface Timing Diagram

TEST SIGNAL



$C_L = 20 \text{ pF}$ for $\bar{E}$
 $C_L = 30 \text{ pF}$ for A0-A15, D0-D7, and $R/\bar{W}$
 $C_L = 50 \text{ pF}$ for all other signals

Figure 2. Signal Loading for Timing Specifications Unless Otherwise Specified

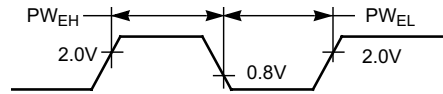
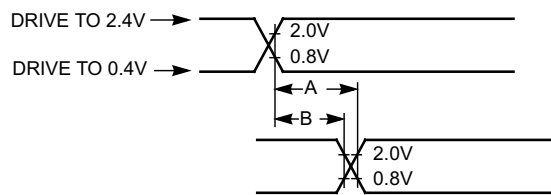


Figure 3. Test Point Levels for $\bar{E}$ Pulse Width Measurements



A — Signal valid-to-signal valid specification (maximum or minimum)
 B — Signal valid-to-signal invalid specification (maximum or minimum)

Figure 4. Drive Levels and Test Point Levels for Timing Specifications Unless Otherwise Specified

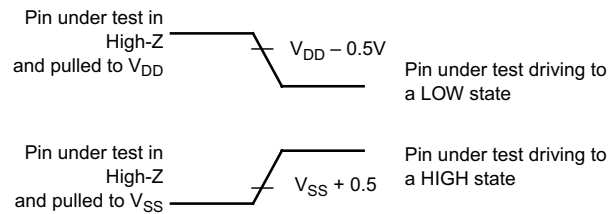


Figure 5. Test Point Levels for High impedance-to-Driven Time Measurements

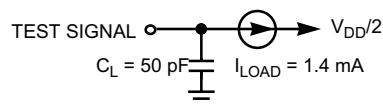
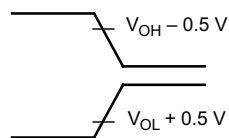


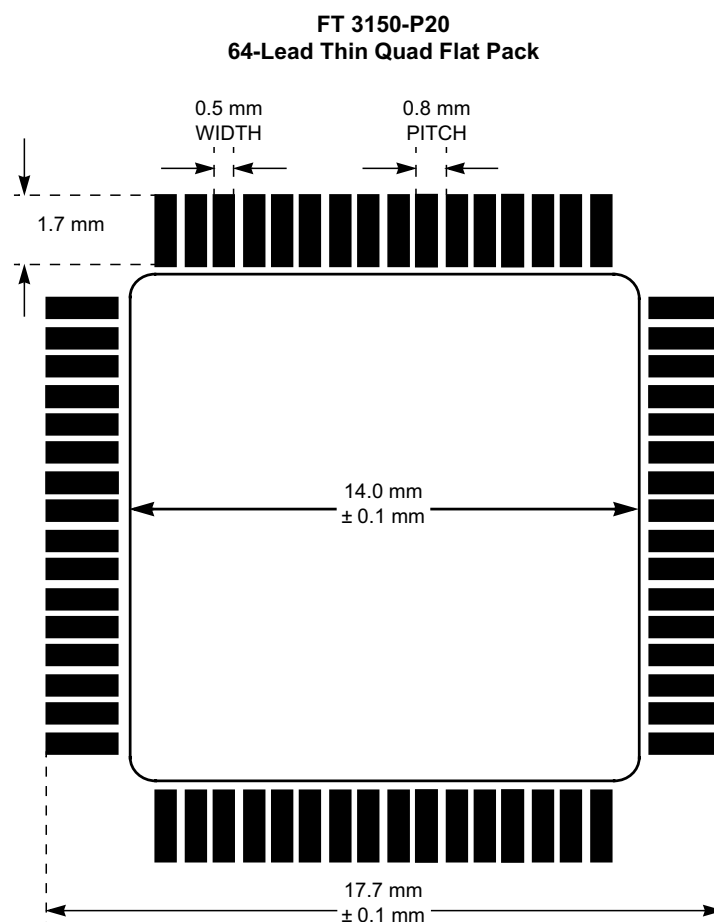
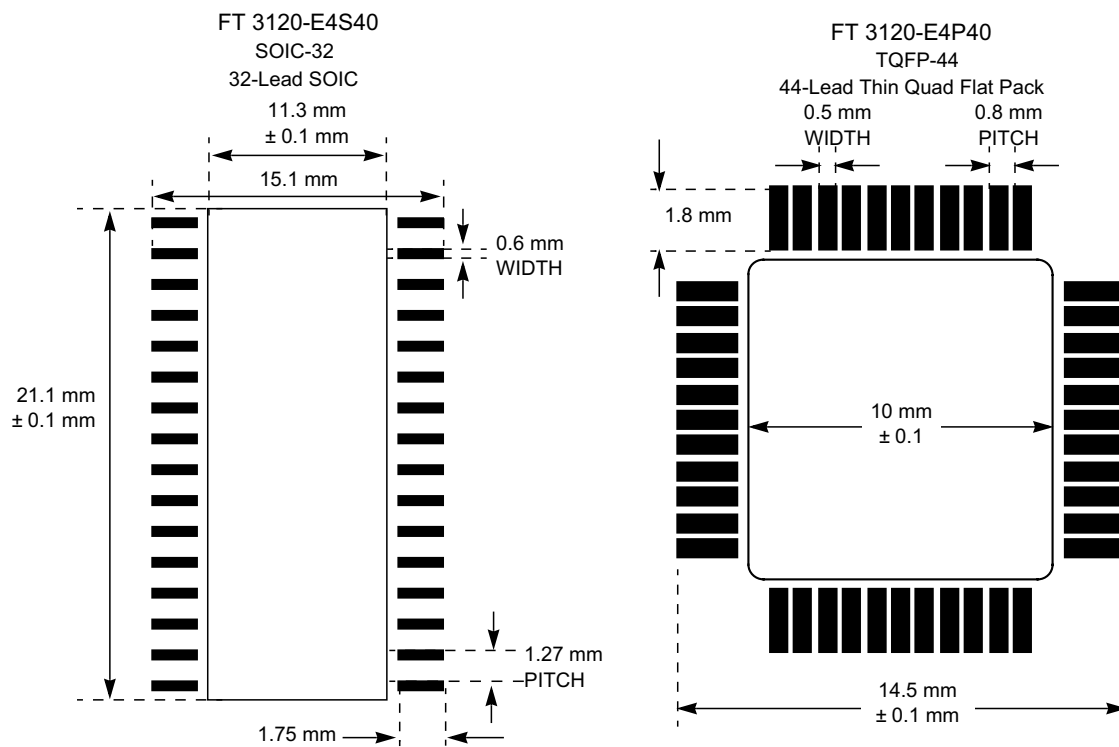
Figure 6. Signal Loading for Driven-to-Three-State Time Measurements



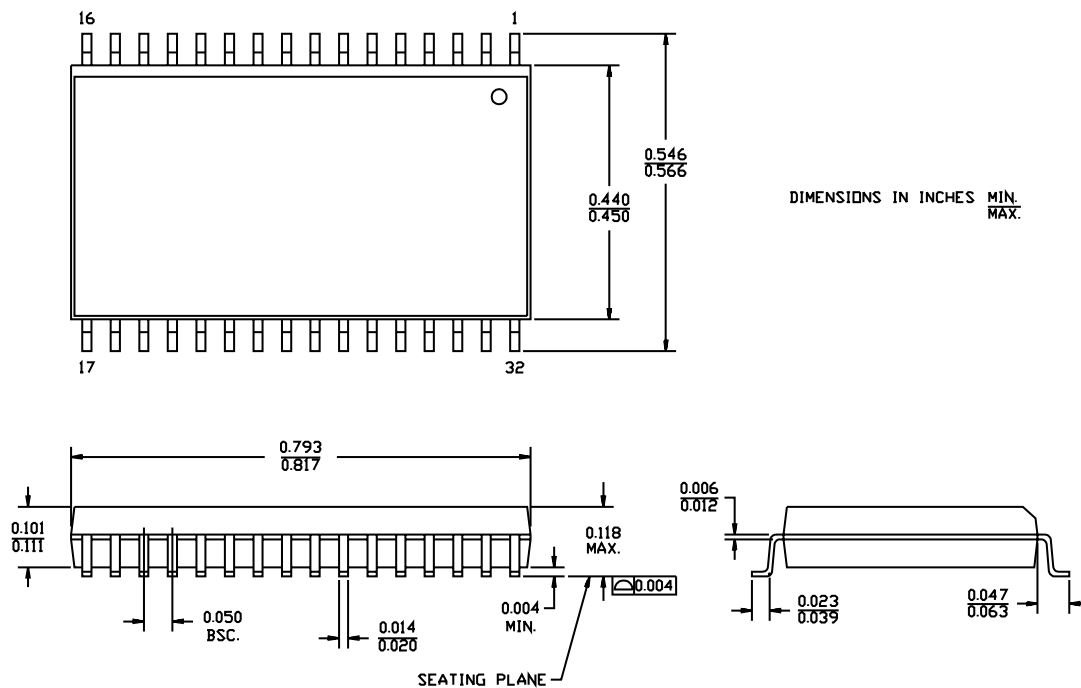
V_{OH} — Measured high output drive level
 V_{OL} — Measured low output drive level

Figure 7. Test Point Levels for Driven-to-High impedance Time Measurements

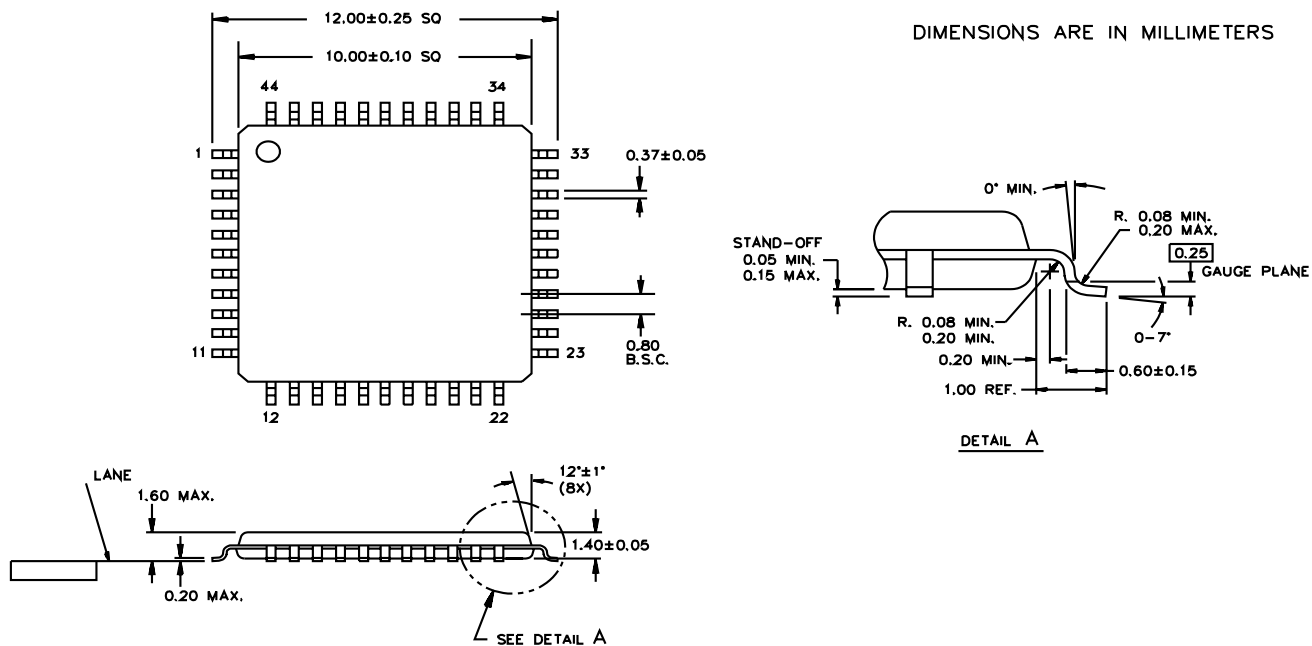
FT 3120 / FT 3150 Smart Transceiver IC Pad Layouts



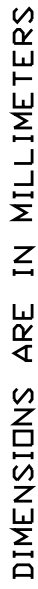
32-Lead (450 MIL) Molded SOIC S34



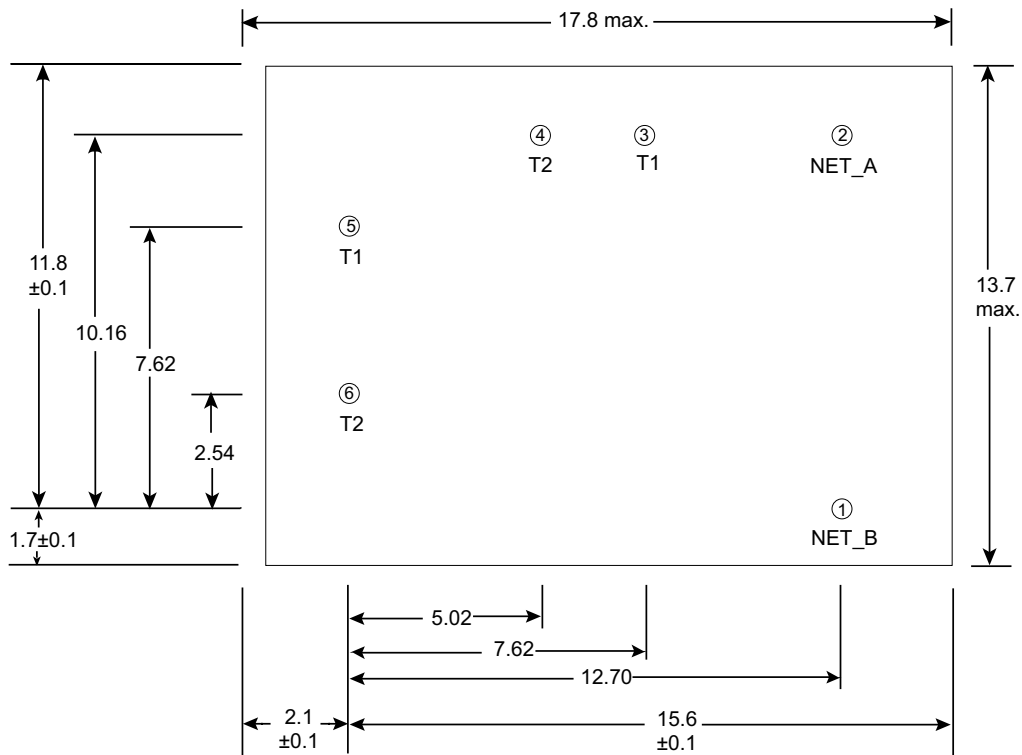
44-Lead Thin Plastic Quad Flat Pack A44



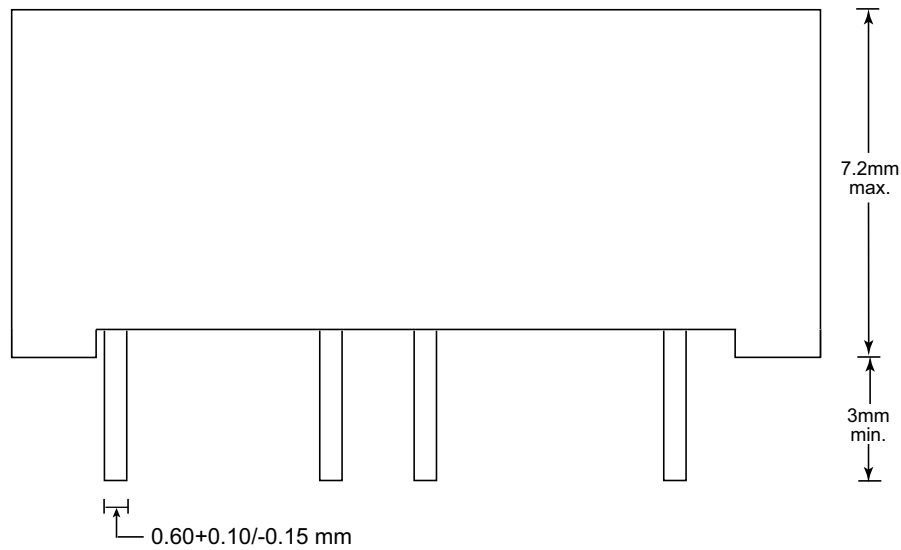
P R E L I M I N A R Y



FT-X1 Communication Transformer^[5] Top View (Dimensions in mm)



FT-X1 Communication Transformer Side View



Network Specifications

Data Communications Type	Differential Manchester coding
Network Polarity	Polarity insensitive
Isolation Between Network and	
0-60Hz, 60 seconds	1000Vrms
0-60Hz, continuous	277Vrms ^[19]
EMI	Designed to comply with FCC Part 15 Level B and EN55022 Level B
ESD	Designed to comply with IEC1000-4-2, Level 4
Radiated Electromagnetic Susceptibility	Designed to comply with IEC1000-4-3, Level 3
Fast Transient/Burst Immunity	Designed to comply with IEC1000-4-4, Level 4
Surge Immunity	Designed to comply with IEC1000-4-5, Level 3
Listings (FT-X1 Communication Transformer)	UL 1950, CSA C22.2 No. 950, TÜV EN60950
Transmission Speed	78 kilobits per second
Number of Transceivers Per Segment	Up to 64
Network Wiring	22 to 16AWG twisted pair; see User's Guide or <i>Junction Box and Wiring Guidelines</i> application note for qualified cable types
Network Length in Free Topology ^[20]	1000m (3,280 feet) maximum total wire with one repeater 500m (1,640 feet) maximum total wire with no repeaters 500m (1,640 feet) maximum node-to-node distance
Network Length in Doubly Terminated Bus Topology ^[20]	5400m (17,710 feet) with one repeater 2700m (8,850 feet) with no repeaters
Maximum Stub Length in Doubly-Terminated Bus Topology	3m (9.8 feet)
Network Termination	One terminator in free topology; two terminators in bus topology (see User's Guide)
Power-down Network Protection	High impedance when unpowered
Physical Layer Repeater	The FT 3120/FT 3150 Smart Transceiver cannot be used to implement a Physical Layer Repeater. In the event that the limits on the number of transceivers or total wire distance are exceeded, FTT-10A transceivers may be used to create Physical Layer Repeaters. See User's Guide for mor details.
Operating Temperature	-40 to 85°C ^[3]
Operating Humidity	25-90% RH @50°C, non-condensing
Non-operating Humidity	95% RH @ 50°C, non-condensing

Notes:

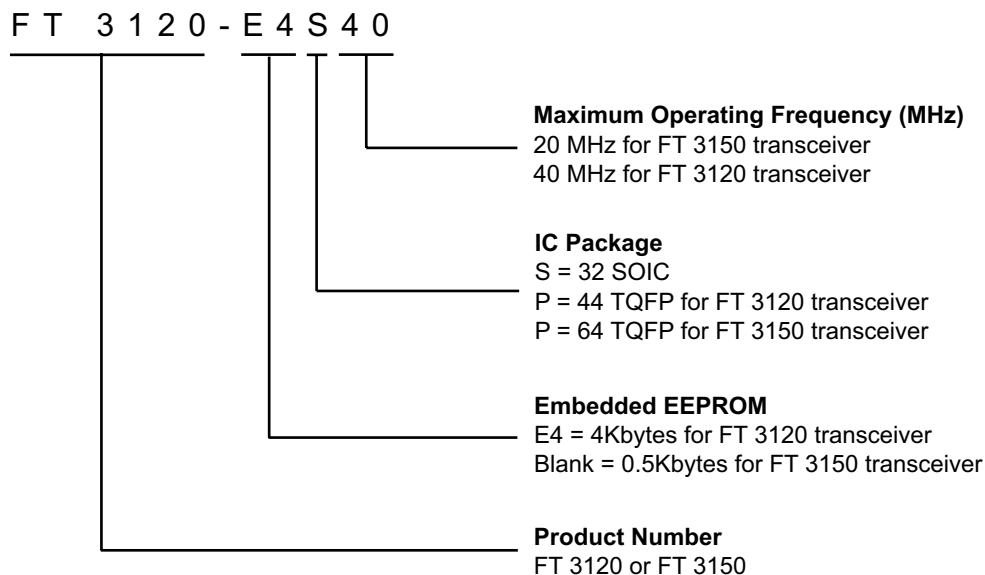
¹⁹ Safety agency hazardous voltage barrier requirements are not supported.

²⁰ Network segment length varies depending on wire type. See User's Guide for detailed specifications.

FT 3120 and FT 3150 Smart Transceiver Ordering Information

Smart Transceiver IC Product Number	Model number	Maximum input clock	EEPROM (Kbytes)	RAM (Kbytes)	ROM (Kbytes)	External memory interface	IC Package
FT 3120-E4S40	14210-500	40MHz	4Kbytes	2Kbytes	12Kbytes	No	32 SOIC
FT 3120-E4P40	14220-900	40MHz	4Kbytes	2Kbytes	12Kbytes	No	44 TQFP
FT 3150-P20	14230-800	20MHz	0.5Kbytes	2Kbytes	N/A	Yes	64 TQFP

Smart Transceiver IC Product Number Description



Communication Transformer Product Number	Model Number	Transformer Package
FT-X1	14240	6-pin through-hole

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