**RFK35N08, RFK35N10**

File Number **1499**

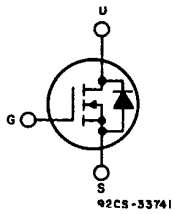
# Power MOS Field-Effect Transistors

# N-Channel Enhancement-Mode Power Field-Effect Transistors

35 A, 80 V - 100 V
$r_{DS}(on)$ = 0.055 Ω

**Features:**
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

**N-CHANNEL ENHANCEMENT MODE**




**TERMINAL DIAGRAM**

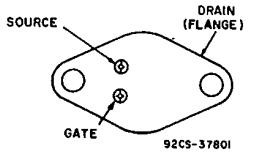
The RFK35N08 and RFK35N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK35N08 and RFK35N10 types were formerly RCA developmental numbers TA9288A and TA9288B, respectively.

**TERMINAL DESIGNATIONS**

RFK35N08
RFK35N10




**JEDEC TO-204AE**

**MAXIMUM RATINGS,** *Absolute-Maximum Values ($T_C$=25° C):*

| | | RFK35N08 | | RFK35N10 | |
|---|---|---|---|---|---|
| DRAIN-SOURCE VOLTAGE | $V_{DSS}$ | 80 | | 100 | V |
| DRAIN-GATE VOLTAGE, $R_{gs}$=1 MΩ | $V_{DGR}$ | 80 | | 100 | V |
| GATE-SOURCE VOLTAGE | $V_{GS}$ | | ±20 | | V |
| DRAIN CURRENT, RMS Continuous | $I_D$ | | 35 | | A |
| Pulsed | $I_{DM}$ | | 100 | | A |
| POWER DISSIPATION @ $T_C$=25°C | $P_T$ | | 150 | | W |
| Derate above $T_C$=25°C | | | 1.2 | | W/°C |
| OPERATING AND STORAGE TEMPERATURE | $T_J$, $T_{stg}$ | | -55 to +150 | | °C |

## RFK35N08, RFK35N10

**ELECTRICAL CHARACTERISTICS,** *At Case Temperature ($T_C$)=25° C unless otherwise specified.*

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | RFK35N08 | | RFK35N10 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $I_D$=1 mA<br>$V_{GS}$=0 | 80 | — | 100 | — | V |
| Gate Threshold Voltage | $V_{GS}(th)$ | $V_{GS}$=$V_{DS}$<br>$I_D$=1 mA | 2 | 4 | 2 | 4 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=65 V<br>$V_{DS}$=80 V | —<br>— | 1<br>— | —<br>— | —<br>1 | μA |
| | | $T_C$=125° C<br>$V_{DS}$=65 V<br>$V_{DS}$=80 V | —<br>— | 50<br>— | —<br>— | —<br>50 | μA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±20 V<br>$V_{DS}$=0 | — | 100 | — | 100 | nA |
| Drain-Source On Voltage | $V_{DS}(on)$[a] | $I_D$=17.5 A<br>$V_{GS}$=10 V | — | 0.9625 | — | 0.9625 | V |
| | | $I_D$=35 A<br>$V_{GS}$=10 V | — | 3.5 | — | 3.5 | V |
| Static Drain-Source On Resistance | $r_{DS}(on)$[a] | $I_D$=17.5 A<br>$V_{GS}$=10 V | — | 0.055 | — | 0.055 | Ω |
| Forward Transconductance | $g_{fs}$[a] | $V_{DS}$=10 V<br>$I_D$=17.5 A | 10 | — | 10 | — | mho |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=25 V<br>$V_{GS}$=0 V<br>f=1 MHz | — | 3000 | — | 3000 | pF |
| Output Capacitance | $C_{oss}$ | | — | 1500 | — | 1500 | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | — | 600 | — | 600 | pF |
| Turn-On Delay Time | $t_d(on)$ | $V_{DD}$=50 V<br>$I_D$=17.5 A<br>$R_{gen}$=$R_{gs}$=50 Ω<br>$V_{GS}$=10 V | 45(typ) | 100 | 45(typ) | 100 | ns |
| Rise Time | $t_r$ | | 225(typ) | 450 | 225(typ) | 450 | ns |
| Turn-Off Delay Time | $t_d(off)$ | | 240(typ) | 450 | 240(typ) | 450 | ns |
| Fall Time | $t_f$ | | 165(typ) | 350 | 165(typ) | 350 | ns |
| Thermal Resistance Junction-to-Case | $R\theta_{JC}$ | RFK35N08, RFK35N10 Series | — | 0.83 | — | 0.83 | °C/W |

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

| CHARACTERISTIC | SYMBOL | TEST CONDITIONS | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | RFK35N08 | | RFK35N10 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Diode Forward Voltage | $V_{SD}$ [a] | $I_{SD}$=17.5 A | — | 1.4 | — | 1.4 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$=4 A<br>$d_{IF}/d_t$=100 A/μs | 200(typ) | | 200(typ) | | ns |

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

## RFK35N08, RFK35N10

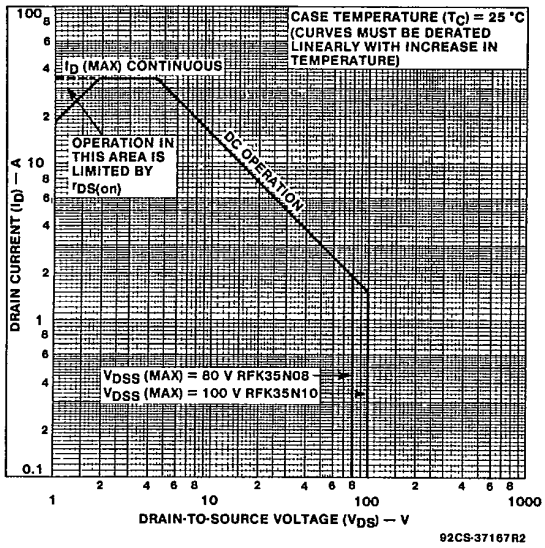



*Fig. 1 — Maximum safe operating areas for all types.*

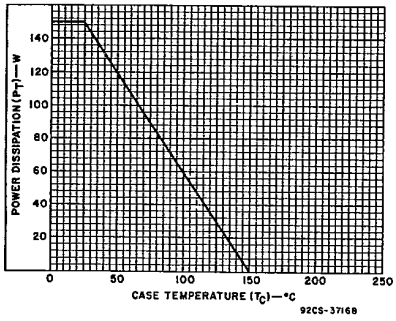



*Fig. 2 — Power vs. temperature derating curve for all types.*

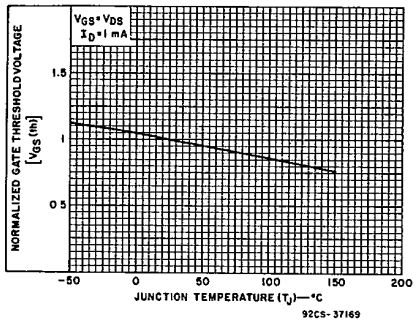



*Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.*

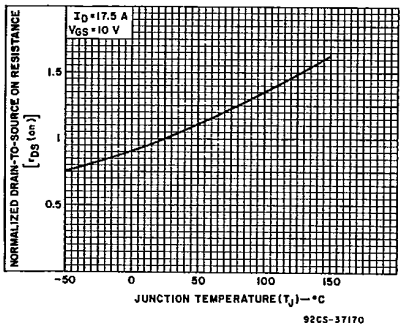



*Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.*

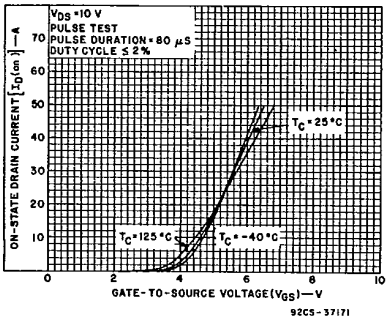



*Fig. 5 — Typical transfer characteristics for all types.*