

## P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
- 30	0.0057 at $V_{GS} = - 10$ V	- 24
	0.0095 at $V_{GS} = - 4.5$ V	- 17

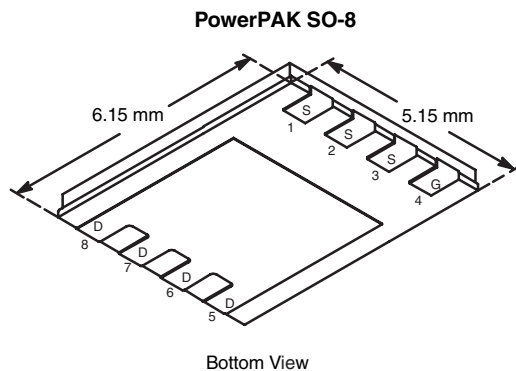
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFETS
- New Low Thermal Resistance PowerPAK<sup>®</sup> Package with Low 1.07 mm Profile
- 100 %  $R_G$  tested



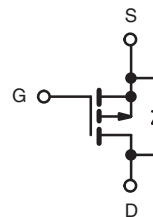
### APPLICATIONS

- Battery and Load Switching
  - Notebook Computers
  - Notebook Battery Packs



Bottom View

Ordering Information: Si7483ADP-T1-E3 (Lead (Pb)-Free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	- 30		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	$T_A = 25$ °C	- 24	- 14	A
		$T_A = 70$ °C	- 19	- 11	
Pulsed Drain Current	$I_{DM}$	- 60			
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	- 4.5	- 1.6		
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25$ °C	5.4	1.9	W
		$T_A = 70$ °C	3.4	1.2	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>b,c</sup>		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{thJA}$	18	23	°C/W
	Steady State		50	65	
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	1.0	1.5	

Notes:

- a. Surface Mounted on 1" x 1" FR4 Board.  
 b. See Solder Profile ( <http://www.vishay.com/ppg?73257> ). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.  
 c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



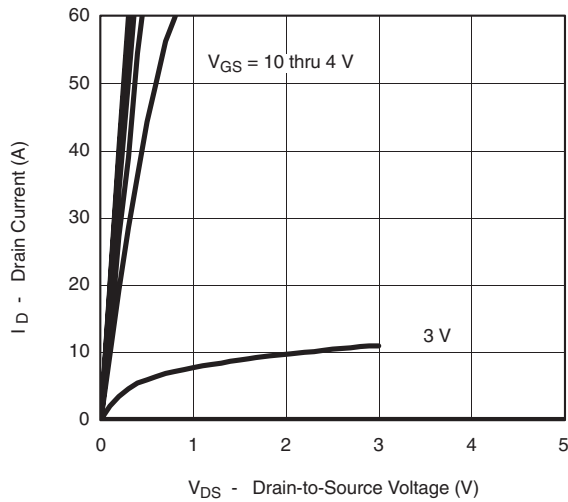
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.0		-3.0	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-30			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -24\text{ A}$		0.0047	0.0057	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -17\text{ A}$		0.0075	0.0095	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -24\text{ A}$		70		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -2.9\text{ A}, V_{GS} = 0\text{ V}$		-0.73	-1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -24\text{ A}$		120	180	nC
Gate-Source Charge	$Q_{gs}$			18		
Gate-Drain Charge	$Q_{gd}$			33		
Gate Resistance	$R_g$		1.6	3.2	4.8	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1.0\text{ A}, V_{GEN} = -10\text{ V}, R_G = 6\text{ }\Omega$		22	35	ns
Rise Time	$t_r$			33	50	
Turn-Off Delay Time	$t_{d(off)}$			210	320	
Fall Time	$t_f$			130	200	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -2.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		70	130	

Notes:

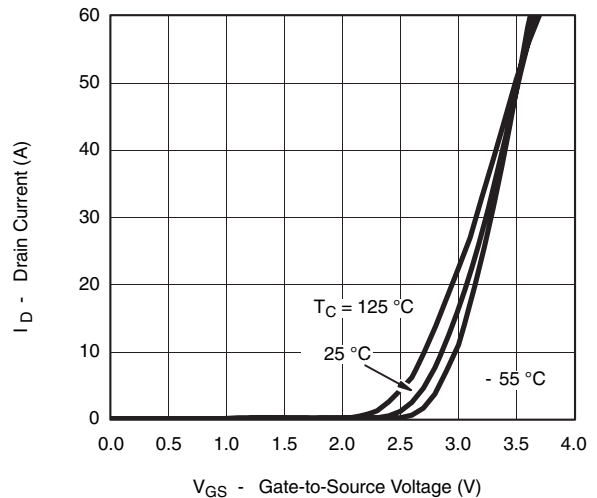
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS**  $25\text{ }^\circ\text{C}$ , unless noted

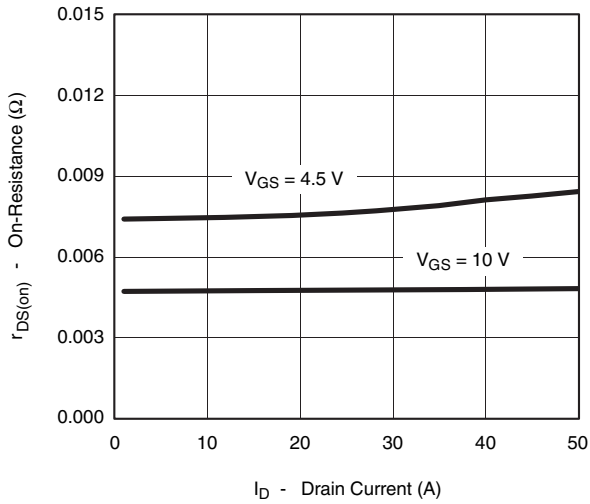


**Output Characteristics**

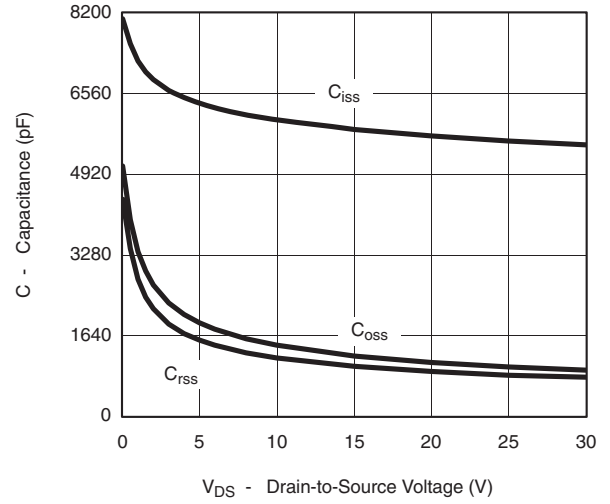


**Transfer Characteristics**

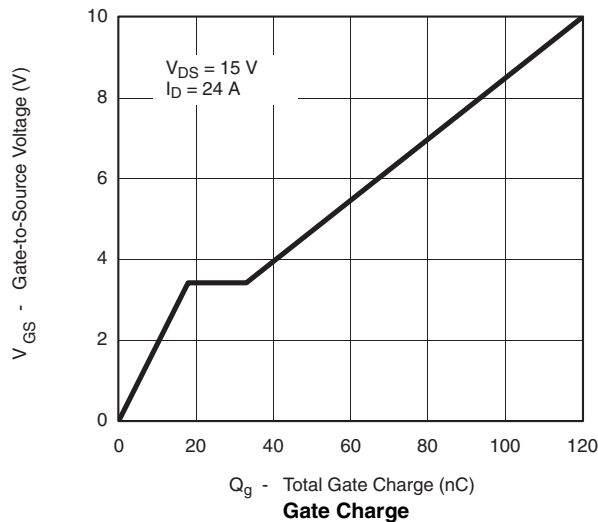
**TYPICAL CHARACTERISTICS** 25 °C, unless noted



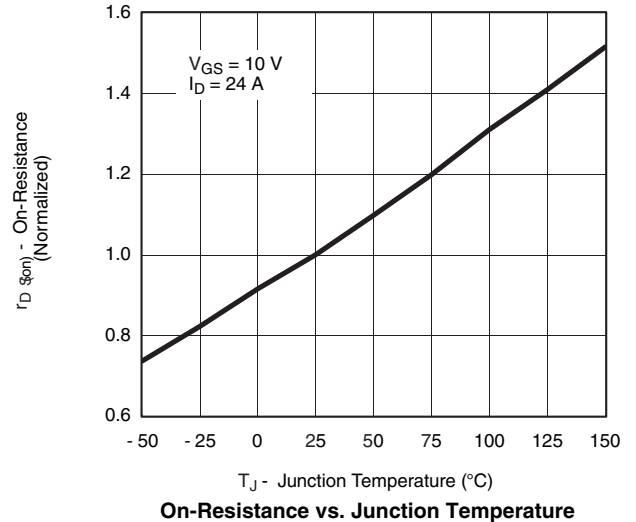
**On-Resistance vs. Drain Current**



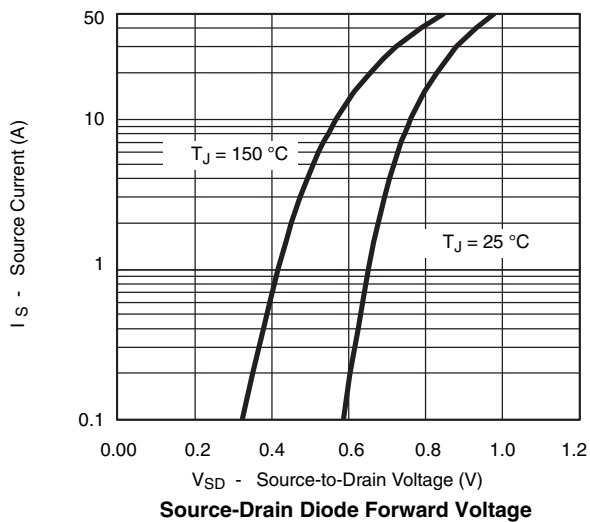
**Capacitance**



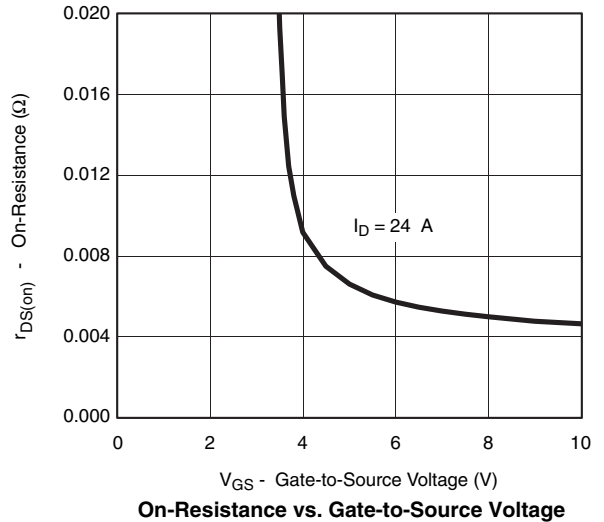
**Gate Charge**



**On-Resistance vs. Junction Temperature**

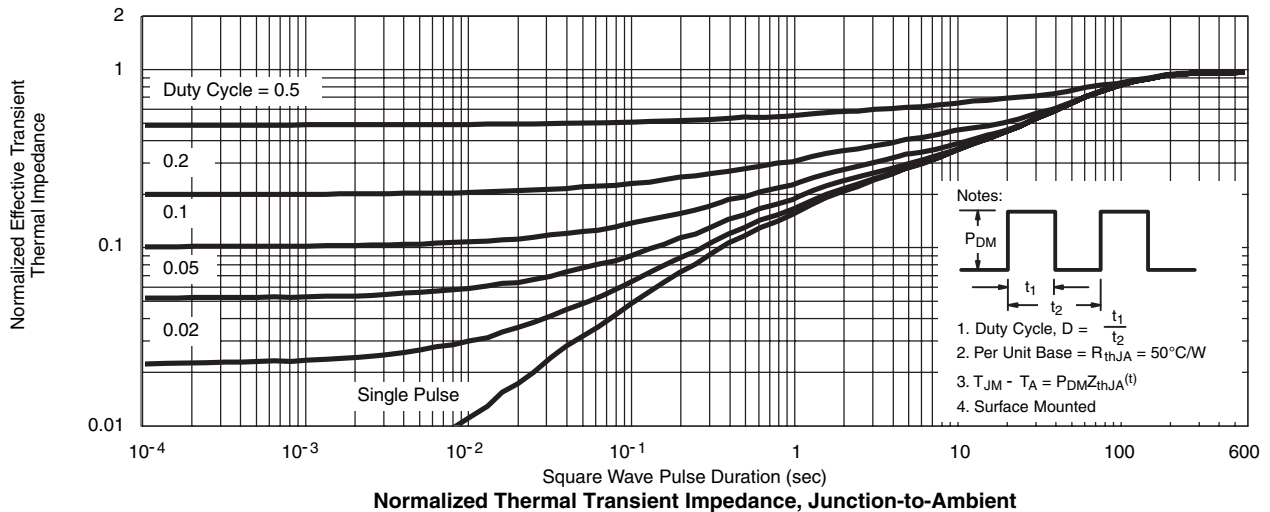
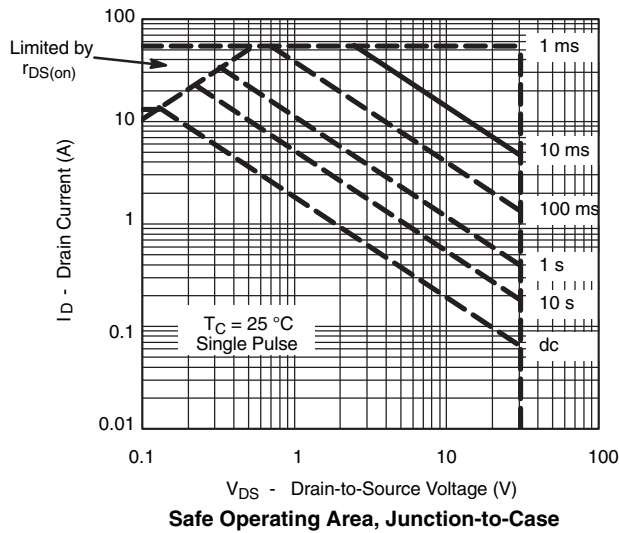
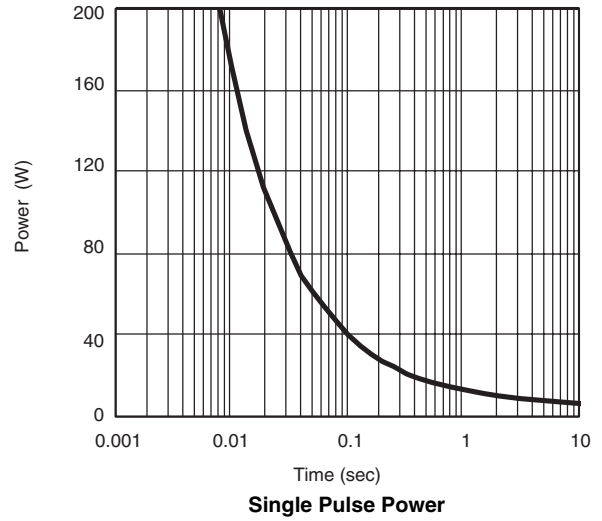
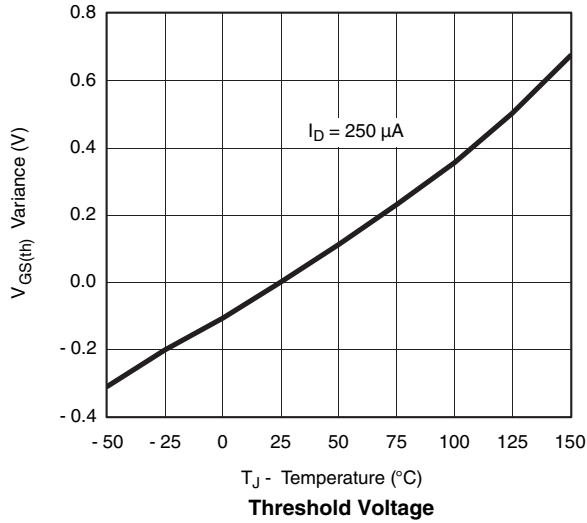


**Source-Drain Diode Forward Voltage**



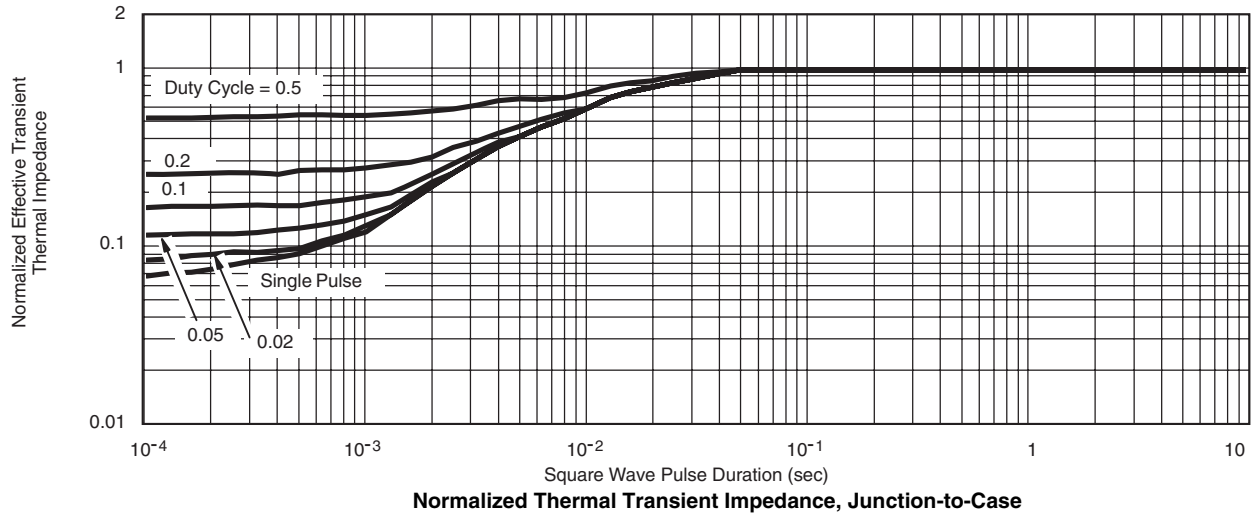
**On-Resistance vs. Gate-to-Source Voltage**

**TYPICAL CHARACTERISTICS** 25 °C, unless noted





**TYPICAL CHARACTERISTICS** 25 °C, unless noted



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