DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128160A CCH-PW-N

1,9”

C-STN-MODULE

Product specification ***Version: 1***

26/SEP /2005

GENERAL SPECIFICATION

MODULE NO. :

DEM 128160A CCH-PW-N

CUSTOMER

VERSION NO.	CHANGE DESCRIPTION	DATE
0	ORIGINAL VERSION	02/02/2005
1	ADDING ROHS VERSION	20/09/2005

PREPARED BY: ZXD DATE: 20/09/2005

APPROVED BY: MH DATE: 20/09/2005

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1. FUNCTIONS & FEATURES

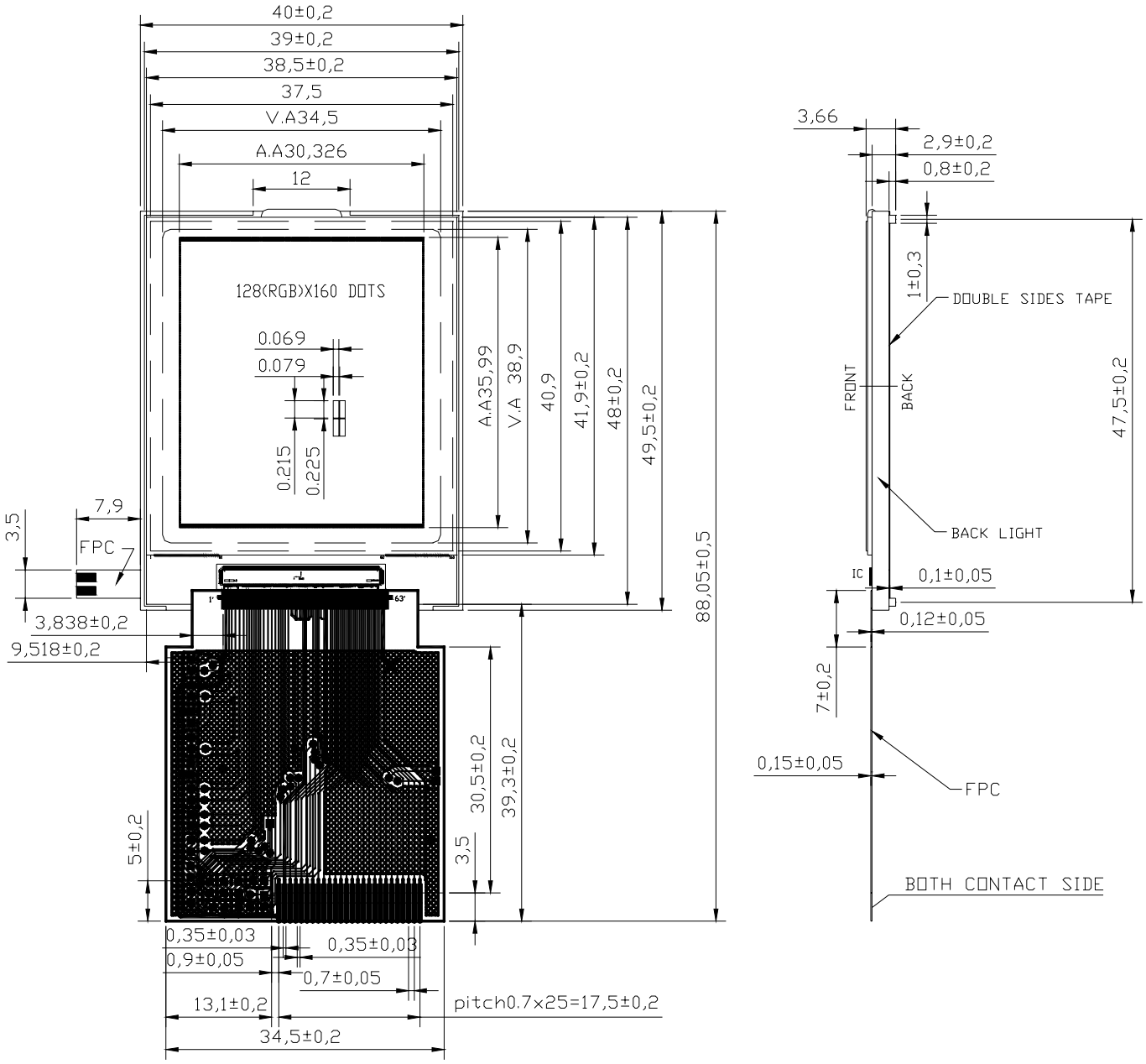
MODULE MODEL	LCD TYPE	POLARIZER TYPE	BACKLIGHT
DEM 128160A CCH-PW-N	C-STN	Transmissive Negative Mode	White LED

- Display Size : 1,9”- COLOR-STN
- Display Color : 65K Color
- IC Type : S6B33B2 (Samsung)
- Viewing Direction : 6 o’clock
- Driving Scheme : 1/162 Duty, 1/7Bias
- Power Supply voltage : 3.0 Volt (typ.)
- Lcd Voltage : 14.4V (typ.)
- Backlight color : White LED-Lightguide
- Operating Temperature : -20°C ~ 70°C
- Storage Temperature : -30°C ~ 80°C

2. MODULE ARTWORK

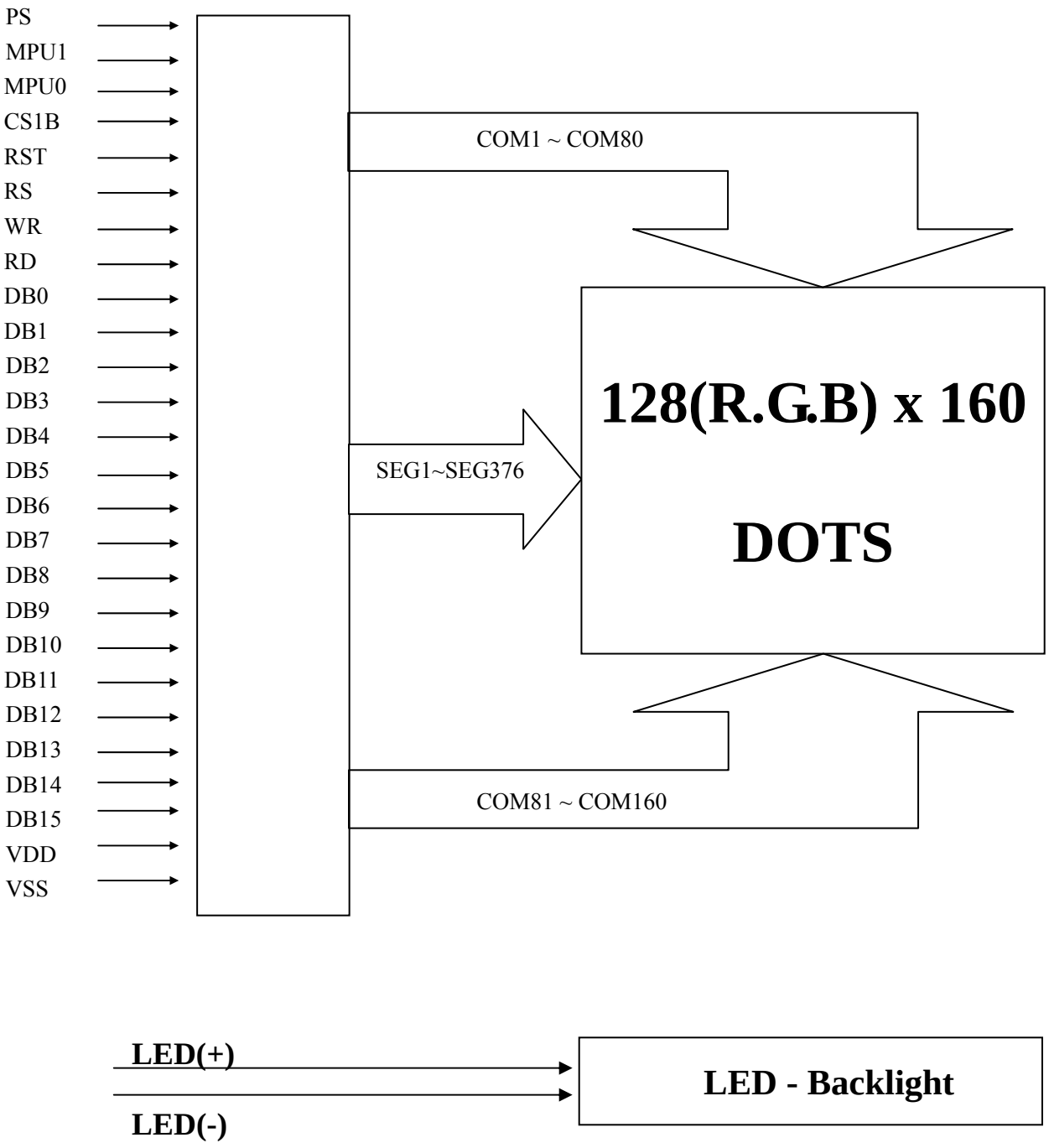
- Module size : 47.9 mm × 88.0 mm × 3.66 mm
- Viewing Area : 34.5 mm × 38.9 mm
- Dot number : 128 × 3 (R.G.B) × 160 DOTS
- Dot Size : 0.215 mm × 0.069 mm
- Dot Gap : 0.010 mm

3. EXTERNAL DIMENSIONS



NOTE:
UNMARKED TOLERANCE IS ±0.30

4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

<table>
<tr><th>Pin NO.</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="8">1~3</td><td rowspan="8">PS
MPU[1:0]</td><td colspan="4">MPU interface select pin</td></tr>
<tr><td>PS</td><td>MPU[1]</td><td>MPU[0]</td><td>Description</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>8080-series 8bit interface</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>8080-series 16bit interface</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>6800-series 8bit interface</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>6800-series 16bit interface</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>3 pin SPI(Write only)</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>4 pin SPI(Write only)</td></tr>
<tr><td>4</td><td>CS1B</td><td colspan="4">Chip select input pins Data / instruction I/O is enabled only when CS1B is “L”. When chip select is non-active, DB0 to DB15 may be high impedance.</td></tr>
<tr><td>5</td><td>RSTB</td><td colspan="4">Reset input pin. When RSTB is “L”, initialization is executed.</td></tr>
<tr><td>6</td><td>D/I
(RS)</td><td colspan="4">Data / Instruction select input pin
− D/I = “H”: DB0 to DB15 are display data
− D/I = “L”: DB0 to DB7 are instruction data</td></tr>
<tr><td rowspan="3">7</td><td rowspan="3">WRB
(R/W)</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>PS</td><td>MPU</td><td>MPU Type</td><td>WRB</td><td>Description</td></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>ReadWRBite control input pin
− R/W = “H”: read
− R/W = “L”: write</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin The data on DB0 to DB15 are latched at the rising edge of the WRB signal.</td></tr>
<tr><td rowspan="3">8</td><td rowspan="3">RDB
(E)</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>MPU[1]</td><td>MPU Type</td><td>RDB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
− R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.
− R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin When RDB is “L”, DB0 to DB15 are in an output status.</td></tr>
<tr><td>9~24</td><td>DB[15:8]
DB[7]/SDI
DB[6]/SCL
DB[5:0]</td><td colspan="4">-DB[15:0]: 16-bit bi-directional data bus.
-SDI: Serial data input pin. The data is latched at the rising edge of SCL.
-SCL: Serial clock input pin.</td></tr>
<tr><td>25</td><td>Vdd</td><td colspan="4">Power supply</td></tr>
<tr><td>26</td><td>Vss</td><td colspan="4">Ground</td></tr>
<tr><td>27</td><td>LED(+)</td><td colspan="4">Power supply voltage for LED</td></tr>
<tr><td>28</td><td>LED(-)</td><td colspan="4">LED GND</td></tr>
</table>

6. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Power supply for logic	VDD-VSS	-0.3 to +3.3	V
Power supply for LCD driver	|VCC – VEE|	22	V
Input Voltage	Vin	- 0.3 to VDD +0.3	V
Operating Temperature range	Top	-20 to +70	°C
Storage Temperature range	Tst	-30 to +80	°C
Led Voltage	Vled	0 to 10.4	V
Current of Led	Iled	0 to 25	mA

7. DC CHARACTERISTICS

7.1 DC CHARACTERISTICS

(Vss = 0V, VDD3 = 1.8 to 3.3V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Operating voltage		VDD3		1.8		3.3	V	VDD3
Operating voltage		VIN1		2.4	-	3.6	V	VIN1,VIN1A
Operating voltage		VIN2		2.4	-	7.2	V	
Operating voltage		VIN45		2.4	-	7.2	V	VOUT45
Operating voltage		DC2IN	1/4 Bias	1.5	-	3.0	V	DC2OUT
			1/5 Bias	1.33	-	2.67		
			1/6 Bias	1.67	-	3.33		
			1/7 Bias	1.5	-	3.0		
Operating voltage		2Vr	2Vr = |(+VR)- (-VR)|	4.0	-	20	V	+VR, -VR
Driving voltage input range		VM	External power supply mode	1.0		2.0	V	VMOUT
		VCC		5.0		12.0	V	VRP
		VEE		-3.0		-8.0	V	VRN
Input voltage	High	VIH		0.8VDD	-	VDD	V	
	Low	VIL		VSS	-	0.2VDD		
Output voltage	High	VOH	IOH = 0.5mA	0.8VDD	-	VDD	V	
	Low	VOL	IOL = 0.5mA	VSS	-	0.2VDD		
Input leakage current		IIL	VIN = VDD or VSS	-1.0	-	+1.0	µA	
Output leakage current		IOZ	VIN = VDD or VSS	-3.0	-	+3.0	µA	
Oscillator Frequency Tolerance	Normal or Partial 0	FOSC1	R1=90kOhm (fFR=100Hz target), DSG=1, 162 display lines	155.5	172.8	190.1	kHz	OSC1 - OSC2
	Partial 1	FOSC2	R1=300kOhm (fFR=77Hz target), 66 display lines	44.35	49.28	54.21	kHz	OSC3 - OSC4
Oscillator Frequency Range	Normal or Partial 0	FOSC1	(*1)	61.44		259.2	kHz	OSC1 - OSC2
	Partial 1	FOSC2	(*2)	29.44		88.32	kHz	OSC3 - OSC4
Driving voltage input range		V1 VM		2.0 1.0	-	4.0 2.0	V	
Regulator output range		REG_OUT	REG_ENB = "L"	1.8	-	2.2	V	

(*1) Minimum oscillator frequency range is defined at fFR=60Hz and display line number=96
Maximum oscillator frequency range is defined at fFR=150Hz and display line number=162

(*2) Minimum oscillator frequency range is defined at fFR=40Hz and display line number=69
Maximum oscillator frequency range is defined at fFR=120Hz and display line number=69

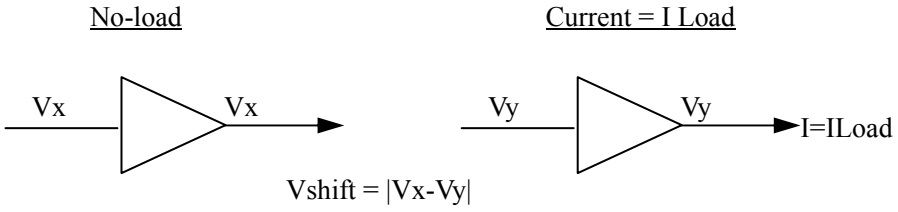
Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	RON-Seg	V1=3.0 V, V0=0V, Ta = 25°C, Iload=50uA	-	1.5	3.0	kΩ	SEGn
	COM	RON-Com	VCC=10.5 V, VM=1.5V, VEE=-7.5V, Ta = 25°C, Iload=100uA	-	1.0	1.5	kΩ	COMn
Current consumption	Normal Mode	IDD	VDD3=VIN1=3.0V, V1=3.0V,Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=162 DSG=1 (No dummy) fOSC1=172.8kHz (fFR=100Hz)Low current mode, No load, No access, All white pattern	-	750	950	µA	VDD3 + VIN1
	Partial1 Mode		VDD3=VIN1=3.0V, V1=3.0V,Bias(2)=1/5, DC(2)=x1.5, Ta=25°C, 1/66 duty fOSC2=49.28kHz (fFR=70Hz)Low current mode, No load, No access, All white pattern	-	300	500	µA	

* : "TBD" is determined from lowest power consumption for dc-dc converter.

(Vss = 0V, VDD3 = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ (+VR)	Isource = 80uA	-	-	150	mV	+VR
	Δ (V1)	Isource = 250uA	-	-	20	mV	V1
	Δ (VM)	Isource,sink = 250uA	-	-	20	mV	VM
	Δ (-VR)	Isink = 80uA	-	-	150	mV	-VR

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
Refer to the following figure. (in case of source current mode)



Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ (+VR)_0 Δ (-VR)_0(*1)	No load	-100	-	+100	mV	+VR -VR

(*1) Tolerance of bias ratio definition
Δ (+VR)_0 = ((+VR) - VM) – VM / Bias
Δ (-VR)_0 = (VM - (-VR)) – VM / Bias

(Vss = 0V, VDD3 = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Remarks
Temperature compensation	ΔVt	VDD3=VIN1=V1=3.0V, -20 to 70 °C		-0.02	-	+0.02	%/°C	V1
Tolerance of Contrast step of V1	ΔVstep			3.13	6.27	9.41	mV	V1
Voltage range	ΔV1 ΔVM	Contrast set = FFh	V1	3.95	4.00	4.05	V	V1
			VM	1.95	2.00	2.05	V	VM
		Contrast set = 00h	V1	1.95	2.00	2.05	V	V1
			VM	0.95	1.00	1.05	V	VM

Item			Condition		Max	Unit	Ref
			Load current	Voltage range			
Offset Voltage	‖+VR-VM‖ -‖VM -(-VR)‖		I Load = +100uA (+VR) I Load = -100uA (-VR)	+VR=5.0~12.0 V V1=2.0~4.0V VM=1.0~2.0V -VR=-3.0~-8.0 V	150	mV	Fig.1
	‖V1-VM‖ -‖VM-V0‖	A	I Load = +100uA (V1, VM)		50	mV	Fig.2
		B	I Load = +100uA (+VR) I Load = -100uA (-VR)				

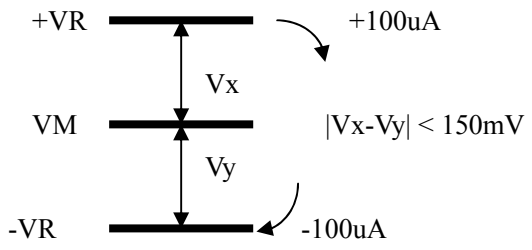


Fig. 1: Offset voltage definition (+VR,VM,-VR)

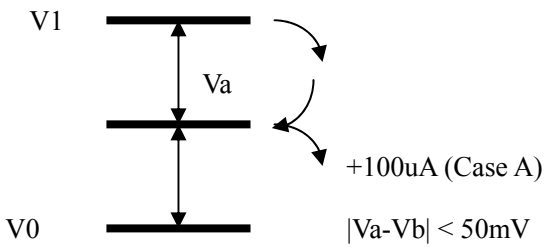
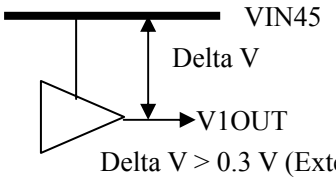


Fig. 2: Offset voltage definition (V1,VM,V0)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

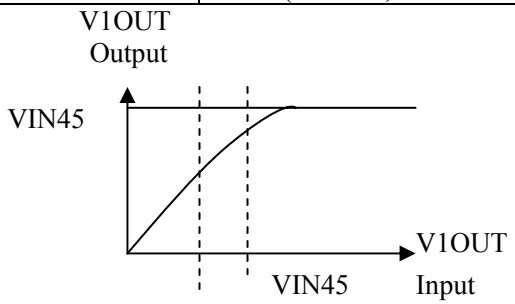
Item		Range	
		Min	Max
Voltage Level	V1OUT	2.0V	4.0 V (DC(1) and DC(2) = X2) (*1)
	VMOUT	1.0V	2.0 V (DC(1) and DC(2) = X2) (*2)
	DC2OUT	1.33V (1/5 Bias, V1OUT = 2V)	3.33V (DC(1) and DC(2) = X2) (*3) (1/6 Bias, V1OUT = 4V)

(*1) This definition is shown as below



Delta V > 0.3 V (External VIN45)

Delta V > 0.5 V (VIN45 = VOUT45)

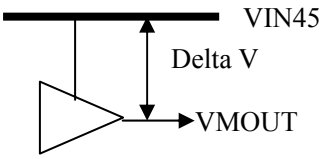


VIN45 - Delta V

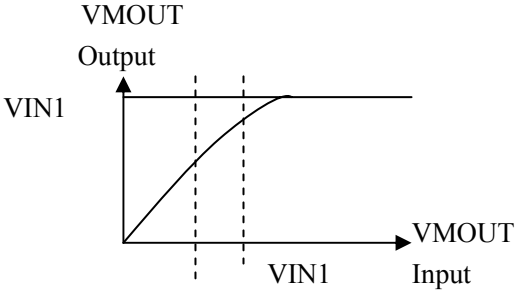
Fig. 1

If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45 .In this case, V1OUT output level must not be unstable. Refer to Fig.1

(*2) This definition is shown as below



Delta v > 0.3V

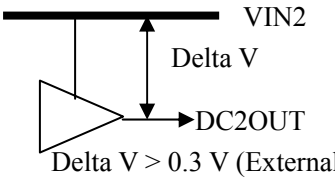


VIN1 - Delta V

Fig.2

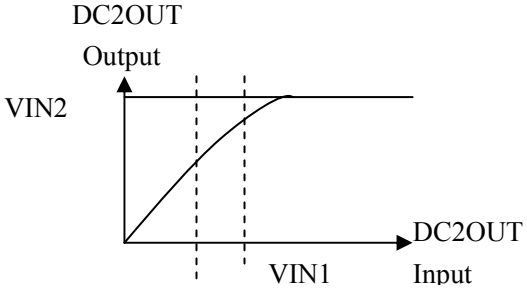
If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped nearVIN1. In this case, VMOUT output level must not be unstable. Refer to Fig.2

(*3) This definition is shown as below



Delta V > 0.3 V (External VIN2)

Delta V > 0.5 V (VIN2 = VOUT45)



VIN2 - Delta V

Fig. 3

If DC2OUT input voltage is set over VIN2, DC2OUT output voltage must be clipped near VIN2. In this case, DC2OUT output level must not be unstable. Refer to Fig.3

7.2 ELECTRICAL CHARACTERISTICS OF BACKLIGHT

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Starting Voltage	Vled	-	10.2	10.4	V	Ta=25°C
Led Current	Iled	-	15	25	mA	Ta=25°C

8. AC CHARACTERISTICS

8-1. Read / Write Characteristics (8080-series MPU)

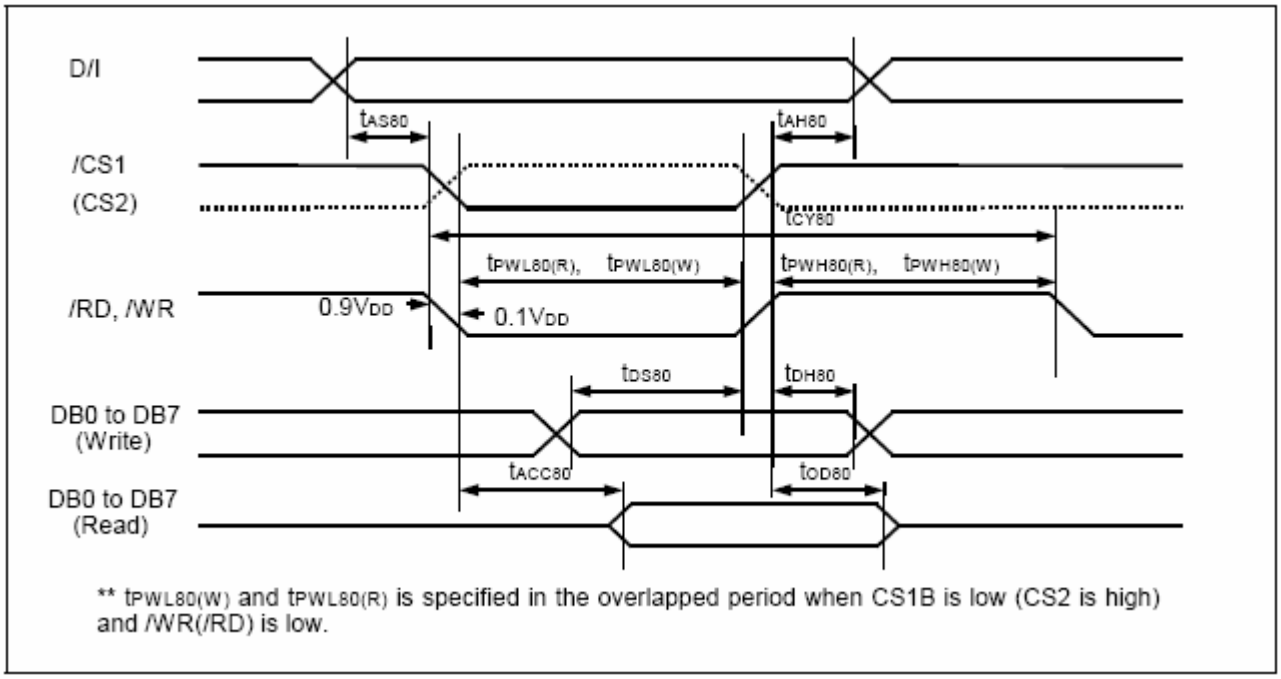


Figure. Parallel Interface (8080-series MPU) Timing Diagram

Table. AC Characteristics (8080-series Parallel Mode)

(V_{DD3} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.		Max.	Unit
				3.3V	1.8V	(3.3V/1.8V)	
Address setup time Address hold time	D/I	t_{AS80} t_{AH80}		0 0	0 0	- -	ns
System cycle time		t_{CY80}		150	360	-	ns
Pulse width low for write Pulse width High for write	WRB (WRB)	t_{PWLW} t_{PWHW}		50 30	100 75	- -	ns
Pulse width low for read Pulse width high for read	RDB (RDB)	t_{PWLR} t_{PWHR}		5 28	10 54	- -	ns
Data setup time Data hold time	DB0 to DB15	t_{DS80} t_{DH80}		-		60 / 120	
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	-		50 / 100	

NOTE:*1. The input signal rise time and fall time (t_r, t_f) is specified at 10 ns or less.

($t_r + t_f$) < (t_{CY80} - t_{PWLW} - t_{PWHW}) for write, ($t_r + t_f$) < (t_{CY80} - t_{PWLR} - t_{PWHR}) for read

8-2. Read / Write Characteristics (6800-series Microprocessor)

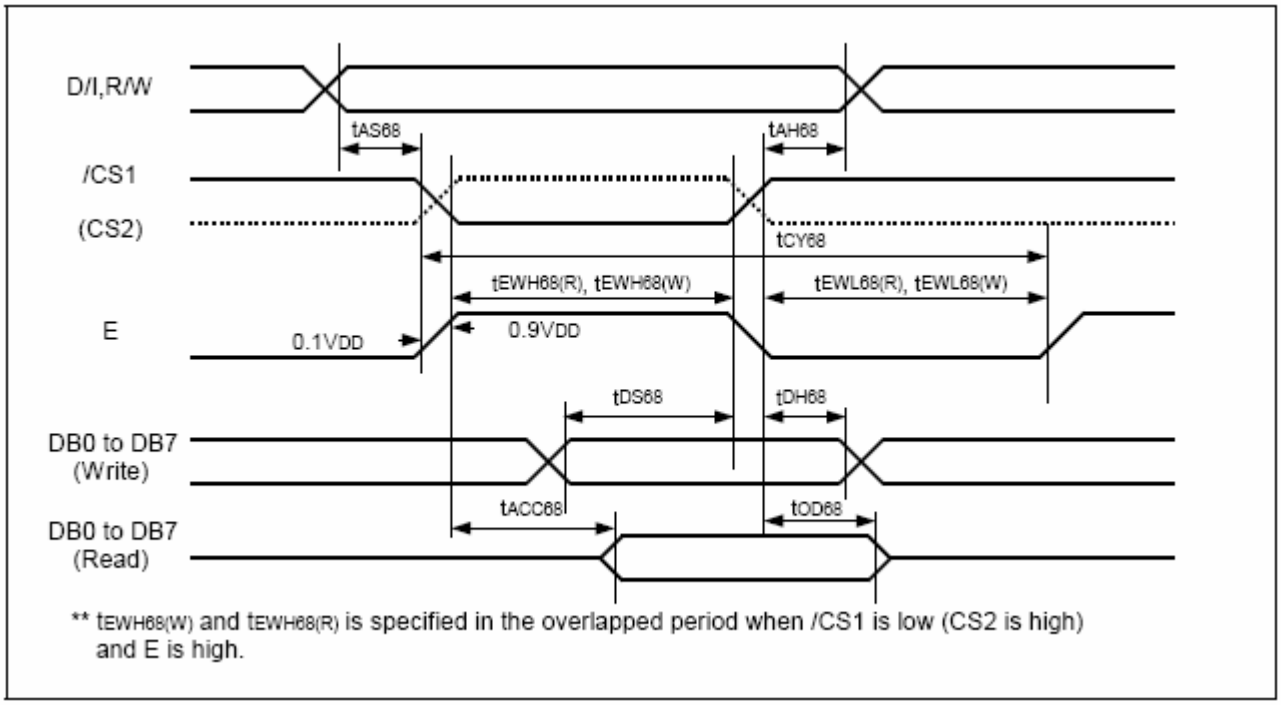


Figure. Parallel Interface (6800-series MPU) Timing Diagram

Table. AC Characteristics (6800-series Parallel Mode)

(V_{DD3} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.		Max.	Unit
				3.3V	1.8V	(3.3V/1.8V)	
Address setup time Address hold time	D/I R/W	t_{AS68} t_{AH68}		0 0	0 0	- -	ns
System cycle time		t_{CY68}		150	360	-	ns
Enable width high for write Enable width low for write	RDB (E)	t_{EWHW} t_{EWLW}		50 30	100 75	- -	ns
Enable width high for read Enable width low for read	RDB (E)	t_{EWHR} t_{EWLR}		5 28	10 54	- -	ns
Data setup time Data hold time	DB0 to DB15	t_{DS68} t_{DH68}		-		60 / 120	
Read access time Output disable time		t_{ACC68} t_{OD68}	CL = 100 pF	-		50 / 100	

NOTE: *1. The input signal rise time and fall time (t_r, t_f) is specified at 10 ns or less.

($t_r + t_f$) < ($t_{CY68} - t_{EWHW} - t_{EWLW}$) for write, ($t_r + t_f$) < ($t_{CY68} - t_{EWHR} - t_{EWLR}$) for read

8-3. Serial Data Interface Timing

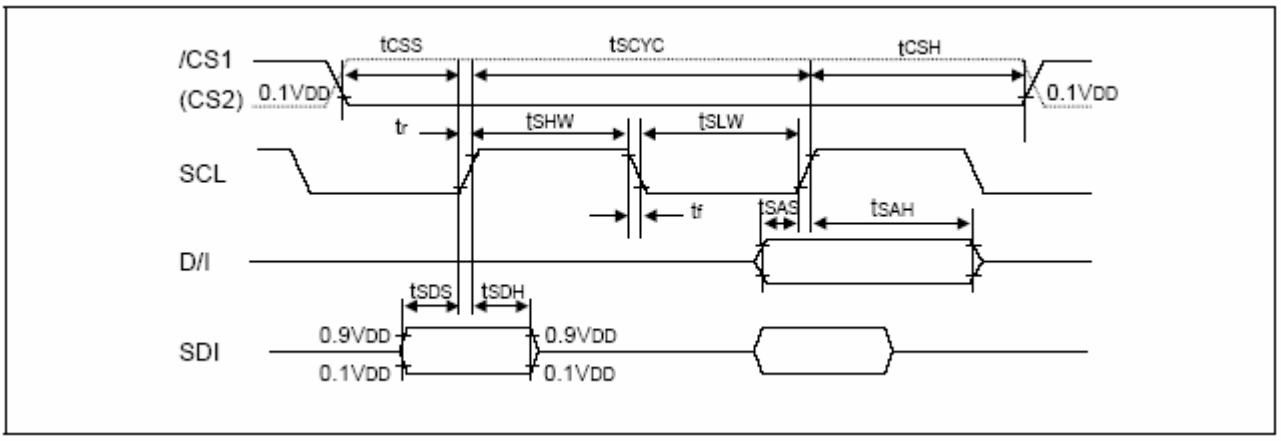


Figure . Serial Interface Timing Diagram

Table . Serial Data Interface Timing

(V_{DD3} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
SCL Cycle Time	SCL	t_{SCYC}		120	-	ns
SCL High Pulse Width	SCL	t_{SHW}		60	-	ns
SCL Low Pulse Width	SCL	t_{SLW}		60	-	ns
SDI Setup time	SDI	t_{SDS}		60	-	ns
SDI Hold time	SDI	t_{SDH}		60	-	ns
D/I Setup time	D/I	t_{SAS}		60	-	ns
D/I Hold time	D/I	t_{SAH}		60	-	ns
Chip Select Setup time	CS1B(CS2)	t_{CSS}		60	-	ns
Chip Select Hold time	CS1B(CS2)	t_{CHS}		60	-	ns

9. OPTICAL CHARACTERISTICS

9.1 OPTICAL CHARACTERISTICS OF LCD

Ta=25°C (Backlight on)

Item			VALUE	Purpose
Chroma	R	X	0.47	preferably
		Y	0.32	
	G	X	0.27	preferably
		Y	0.44	
	B	X	0.15	preferably
		Y	0.12	
Lighteness	R		16.3	OK
	G		35.1	OK
	B		15.1	OK

Item	Test Condition	Fact	Purpose
Response Time(Tr+Td)	@25°C(mS)	280+180	OK
	@-10°C(mS)	1120+920	OK
Contrast(Max)	@25°C 14.5V	46	OK
Viewing Cone	Direction	Color display angle of view	
	6:00	50°	OK
	9:00	40°	OK
	12:00	42°	OK
	3:00	50°	OK

9.2 OPTICAL CHARACTERISTICS OF BACKLIGHT

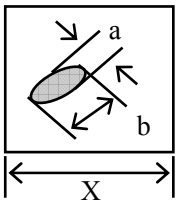
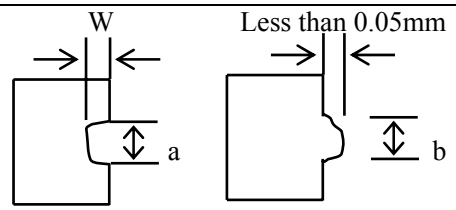
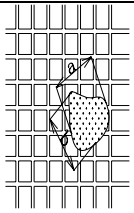
Item	Min.	Typ.	Max.	Unit
Brightness	2200	2536	2678	cd/㎡
Uniformity	80	-	90	%

10. QUALITY ASSURANCE

10-1. Electric Characteristic

No.	Item	Judgement Criteria
1	No indicate	NO - GO
2	Miss-operation	NO - GO
3	Partially	NO - GO
4	Contrast non-uniform	Notable non-uniform is not allowed
5	Contrast	According to specification
6	Response speed	According to specification

10-2. Light-On Outline

No.	Item	Judgement Criteria
1	Dot Pin Hole	 (Ⅰ)(a+b)/2≤ 0.4X (Ⅱ)Tolerance dots:7 dots (but not concentration) Remark:X=Segment wide
2	Dot deform	 (Ⅰ) a,b≤ 0.5X,W≤ 0.3X (Ⅱ) Can not be short
3	Dot too fat/thin	Dot width ≤ ±15%
4	Defect of aligning	

Φ grain size (mm)	Tolerance Dots
Φ≤ 0.5	neglect
0.5 < Φ≤ 1.0	5
1.0 < Φ≤ 1.5	3
1.5 < Φ≤ 2.0	2

(Ⅰ) Φ grain size showed by (a+b)/2

(Ⅱ) Allowed Dots : 7 Dots.

10-3. LCD Panel Outline

<table>
<tr><th>No.</th><th>Item</th><th>Judgement Criteria</th></tr>
<tr><td>1</td><td>Panel
(include polarizer, reflector)

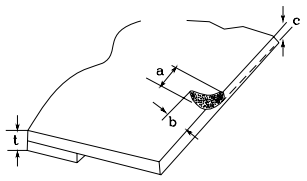
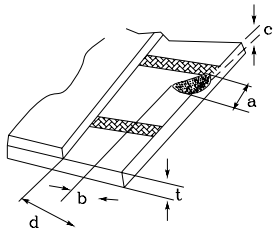
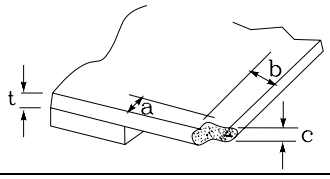
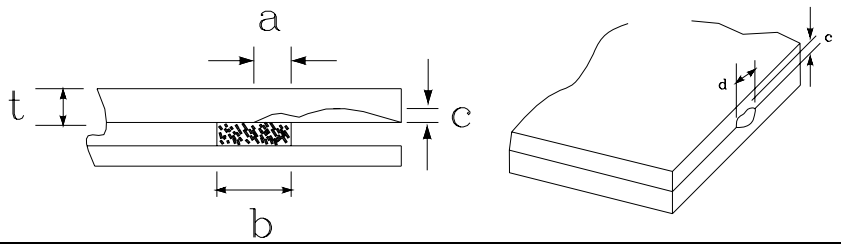
Black spots,
White spots,
Fiber,
Scratch,
Space concentration,</td><td>(1) Black Spots/White Spots

<table>
<tr><td>Φ grain size (mm)</td><td>Tolerance Dots</td></tr>
<tr><td>Φ ≤ 0.10</td><td>neglect</td></tr>
<tr><td>0.10 < Φ ≤ 0.15</td><td>3</td></tr>
<tr><td>0.15 < Φ ≤ 0.20</td><td>3</td></tr>
<tr><td>0.20 < Φ ≤ 0.25</td><td>1</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
(Ⅰ) Φ grain size:
(Iong diameter + short diament) /2 = average diameter
(Ⅱ) for more defect condition , Total quantity of spots : 5 pcs
(Ⅲ) for more defect condition , partition distance must over 5mm

(2) Line Defect

<table>
<tr><td colspan="2">Φ grain size (mm)</td><td rowspan="2">Tolerance Dots</td></tr>
<tr><td>Length</td><td>Wide</td></tr>
<tr><td>Φ ≤ 2.0</td><td>Φ ≤ 0.02</td><td>neglect</td></tr>
<tr><td>2.0 < Φ ≤ 3.0</td><td>0.02 < Φ ≤ 0.04</td><td>5</td></tr>
<tr><td>3.0 < Φ ≤ 4.0</td><td>0.04 < Φ ≤ 0.05</td><td>2</td></tr>
<tr><td>4.0 < Φ</td><td>0.05 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>2</td><td>Scratch ,Glass
Polarizer , Reflector</td><td>Follow the above NO.1 (2) Line Defect.</td></tr>
<tr><td>3</td><td>Bubble , Polarizer , Reflector</td><td>
<table>
<tr><td>Φ grain size (mm)</td><td>Tolerance Dots</td></tr>
<tr><td>Φ ≤ 0.3</td><td>neglect</td></tr>
<tr><td>0.3 < Φ ≤ 0.5</td><td>3</td></tr>
<tr><td>0.5 < Φ ≤ 1.0</td><td>1</td></tr>
<tr><td>1.0 < Φ</td><td>0</td></tr>
</table>
(Ⅰ) Φ grain size = average diameter</td></tr>
</table>

10-4. General Outline

No.	Item	Judgement Criteria
1	Glass Crack	Panel Spec : (Ⅰ) a, b≦ 0.5(mm) , neglect. (Ⅱ) a≦ 5(mm) or the length less of crack is 10% than panel length , the criteria follow stricter. (Ⅲ) b≦ 2(mm) , c≦ t. (Ⅳ) Follow above , the allowed dots≦ 2 dots. 
2	Panel cracks ITO terminal	Panel Spec : (Ⅰ) a≦ 2(mm). (Ⅱ) b≦ 25% of d , And c≦ t. (Ⅲ) Follow above , the allowed cracks≦ 2 cracks. (Ⅳ) 2 continuous cracks at panel are not allowed.  Panel Spec : (Ⅰ) a≦ 2mm, b≦ 1/3 ITO terminal and c≦ t (Ⅱ) a : length can not crack to ITO . 
3	Seal side crack	Panel Spec : (Ⅰ) a≦ b/3, c≦ t/2, d≦ 3mm, and b is width of seal. (Ⅱ) Follow above, The allowed cracks≦ 2 cracks . 

11. RELIABILITY TEST

Operating life time: Longer than 50000 hours

(at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

TEMPERATURE TESTS	NORMAL GRADE
High temperature storage	+70°C *96hrs (Without Polarizer)
Low temperature storage	-30°C* 4hrs
High temperature operation	+60°C *96hrs
Low temperature operation	-20°C *4hrs
High temperature, High humidity	+60°C* 95%RH *96hrs (Without Polarizer)
Thermal shock	-20°C *30min. 10s ↓ 5Cycles +60°C *30min.
Vibration test	Frequency *Swing * Time 40Hz * 4mm * 4hrs
Drop test	Drop height*Times 1.0m * 6times

12. LCD MODULES HANDLING PRECAUTIONS

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

13. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections.