## DISPLAY Elektronik GmbH

# DATA SHEET

2,2" TFT MODULE

**DEM 240320A TMH-PW-N** 

**Product Specification** 

Version: 5.0

21.May 2008

REVISION	N HISTORY:			
Revision	Date	Description	Written By	Approved By
1.0	15-Jun-2007	New Release	ХН	МН
2.0	28-Apr2008	<ol> <li>Change the command table and add the IC version in item 6.0.</li> <li>Correct the location of lot number.</li> </ol>	ХН	МН
3.0	8-May2008	<ol> <li>Updated the module drawing.</li> <li>Modify item 10.0.</li> </ol>	ХН	МН
4.0	15-May2008	<ol> <li>Correct the pin assignment</li> <li>Update the pin description</li> </ol>	XH	МН
5.0	21-May2008	Change the interface description	XH	МН

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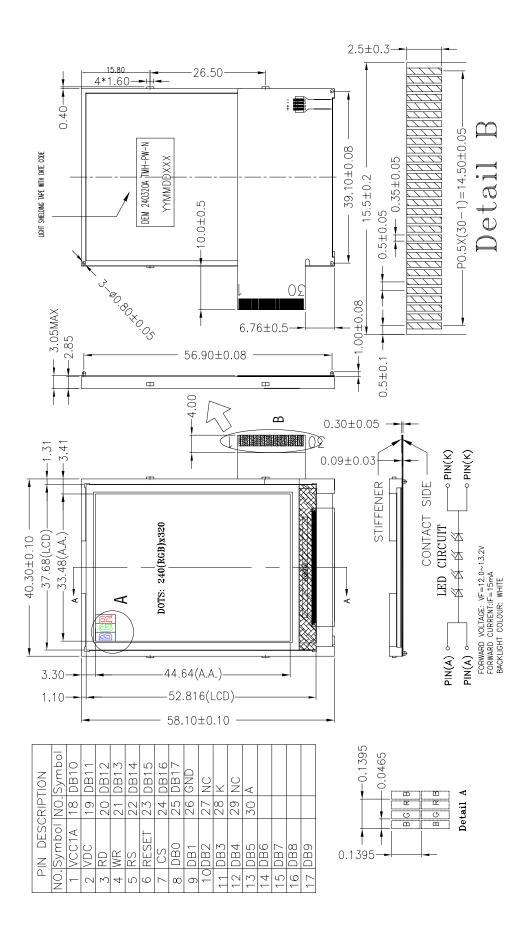
## 1.0 GENERAL SPECIFICATION

Item	Contents	Unit
LCD Type	2.2 inch a-Si TFT active-matrix Transmissive	-
Module outer dimension	40.30 x 58.10 x 3.05	mm
Pixel Size	0.1395(RGB) x 0.1395	mm
Active display area	33.48 × 44.64	mm
Number of dots	240(RGB) x 320	dots
Viewing direction	6	O'clock
Color-filter-array	RGB Stripe	
Number Of Colors	262k	
Backlight	LED white backlight	-
Drive IC	HX8346-A (HIMAX)	-
Interface type	16-bit 80 mode.	See Note
Operating temperature	-20 ~ 70	°C
Storage temperature	-30 ~ 80	°C
Weight	~ 10	g

Note: Below interfaces can be custom-made according to different applications:

- 8/18-bit MPU (68-system and 80-system) parallel interface, 16-bit 68-system parallel interface
- 3-wire serial data transfer interface
- 16, 18 data lines parallel video (RGB) interface.

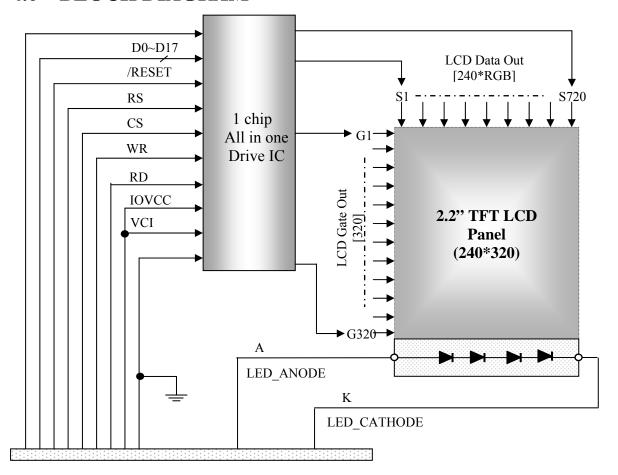
## 2.0 OUTLINE DRAWING



## 3.0 INTERFACE PIN DESCRIPTION

Pin No.	Symbol	Function					
1	V <sub>CC</sub> 1A	Logic power supply.					
2	VDC	Power supply.					
3	RD	Read strobe signal.					
4	WR	Write strobe signal.					
5	RS	Register selection input					
		When RS = "low", instruction register.					
		When RS = "high" . data register .					
6	RESET	Reset signal.					
7	CS	Chip select signal. Low active.					
8 ~ 25	DB0 ~ DB17	Data Bus.					
26	GND	Power ground.					
27	NC	No connection.					
28	K	Cathode of the backlight power supply.					
29	NC	No connection.					
30	A	Anode of the backlight power supply.					

## 4.0 BLOCK DIAGRAM



#### **5.0 OPERATING PRINCIPLE & DRIVING METHOD**

- Please refer to HX8346-A(T)-V01 datasheet for more details.
- Instruction Description (based on IC spec ver as stated in 6.1 where the product is 5.2 designed). This instruction description is for reference only. Customer is encouraged to always refer to the latest IC specification.

Register	Bantafaa	MUD.		Upper				Low	er Code				Comment
No.	Register	W/R	RS	D[23:8]	D7	De	D5	D4	D3	D2	D1	D0	Comment
R01h	Display Mode control	W/R	1						IDMON (0)	INVON (0)	NORON (1)	PTLON (0)	
R02h	Column address start 2	W/R	1					SC[1:	5:8] (8160)	1-1	1-7		
R03h	Column address start 1	W/R	1					SC[7	(101'8) [O:				
R04h	Column address end 2	W/R	1					EC[1	5:8] (8160)				
R05h	Column address end 1	W/R	1					EC[7:0] (8	rb1110_1111	1)			
R06h	Row address start 2	W/R	1					SP[15	5:8] (8'b0)				
R07h	Row address start 1	W/R	1			SP[7:0] (6'b0)							
R08h	Row address end 2	W/R	1					EP[15:8] (	8.P0000 <sup>0</sup> 000	1)			
R09h	Row address end 1	W/R	1					EP[7:0] (8	3'b0011_1111	1)			
ROAh	Partial area start row 2	W/R	1					PSL[1	5:8] (8'60)				
ROBh	Partial area start row 1	W/R	1					PSL[7	7:0] (8'b0)				
ROCh	Partial area end row 2	W/R	1			PEL[15:8] (8'b0000_0001)							
RODh	Partial area end row 1	W/R	1					PEL[7:0] (	8'b0011_111	1)			
ROEh	Vertical Scroll Top fixed area 2	W/R	1					TFA[1	5:8] (8'60)				<u></u>
ROFh	Vertical Scroll Top fixed area 1	W/R	1					TFA[	7:0] (8 <b>'b</b> 0)				
R10h	Vertical Scroll height area 2	W/R	1					VSA[15:8]	8'b0000_000	11)			
R11h	Vertical Scroll height area 1	W/R	1					VSA[7:0] (	8'b0011_111	1)			
R12h	Vertical Scroll Button area 2	W/R	1					BFA[1	5:8] (8'b0)				
R13h	Vertical Scroll Button area 1	W/R	1			BFA [7:0] (8'b0)							
R14h	Vertical Scroll Start address 2	W/R	1					VSP [1	5:8] (8d'0)				
R15h	Vertical Scroll Start address 1	W/R	1			VSP [7:0] (8d'0)							
R16h	Memory Access control	W/R	1		MY(0)	MX(0)	MV(0)	•	BGR(0)				
R18h	Gate Scan and Scroll control	W/R	1					7.			SCROLL EN(0))	SM(0)	
R19h	OSC Control 1	W/R	1	. (				OSCADJ[	5:0] (10_000	0)	_	OSC E N(1)	
R1Ah	OSC Control 2	W/R	1	Sir	7 . 1	-7	<u> </u>	•				OSC TEST(0)	
R1Bh	Power Control 1	W/R	b	V	NISDENB (0)	11		PON(0)	DK(0)	XDK(0)	VLCD TRI(0)	STB(1)	
R1Ch	Power Control 2	W/R	30	25							AP[2:0] (100)		
R1Dh	Power Control 3	WR	11				VC2[2:0] (100)	)			VC1[2:0] (100)		
R1Eh	Power Control 4	W/R	Y		$( \cdot )$			•			VC3[2:0] (000)		
R1Fh	Power Control 5		Ĺ.,		1			-		VRH[3:	:0] (0110)		
R20h	Power Control 6	W/R	1 '	11.	_	ВТ[3:0	] (0100)				•		
R21h	Power Control 7	W/R	1	· · ·	· ·		FS1[1:	0] (11)			FS0[1:0	] (00)	
R22h	SRAM Write Control	W/R	1					SRAM Wr	ite .				
R23h	Cycle Control 1	W/R	1					N_DC[7:0	] (1001_0101	1)			
R24h	Cycle Control 2	W/R	1					P_DC[7:0]	] (1001_0101	1)			
R25h	Cycle Control 3	W/R	1						(1111_1111				
R26h	Display Control 1	W/R	1		PT[1:	0] (10)	GON(1)	DTE(0)	D[1:	0] (00)			
R27h	Display Control 2	W/R	1								0] (4'b0010)		
R28h	Display Control 3	W/R	1								0] (4'b0010)		
R29h	Display Control 4	W/R	1		P_BP[3;0] (4'00010)								
R2Ah	Display Control 5	W/R	1		P_FP(3:0] (4b0010)								
R2Ch	Display Control 6	W/R	1			I_BP[3:0] (4'b0010)							
R2Dh	Display Control 7	W/R	1			I_FP[3:0] (4'b0010)							
R2Fh	Display Control 8	W/R	1					Version i	D (read only)	)			

Regist	Register	WR	RS	Upper Code				Lower C	ode				Comment
erNo.	Lagiora	****	11.0	D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Comment
R30h	Display Control 9	W/R	1							SAPS1[3:	0] (1000)		
R37h	Display Control 16	W/R	1			-	PTG[1	:0] (00)		ISC[3:0]			
R38h	RGB Interface control 1	W/R	1					RGB_	DPL	HSPL	VSPL	EPL	
R3Ah	Cycle Control 1	W/R	1			N RTN[3:0]	(0000)	EN(0)	(0)	(D) N	(0) NW[2:0] (00	(0)	
R3Bh	Cycle Control 2	W/R	1			P_RTN[3:0]	<u> </u>				NW[2:0] (00		
R3Ch	Cycle Control 3	W/R	1			I RTN[3:0] (					NW[2:0] (00		
R3Dh	Cycle Control 4	W/R	1								DIV[1	:0] (00)	
R3Eh	Cycle Control 5	W/R	1			SON[7:0] (8b0011_1000)							
R40	Cycle Control 6	W/R	1					ON[7:0] (8'b0					
R41h	Cycle Control 7	W/R	1					OF[7:0] (8'b1	111_1000)				
R42h	BGP Control	W/R	1		1/20140			•		BGP[3:0	] (1000)	Г	
R43h	VCOM Control 1	W/R	1		VCOMG (1)					$\mathcal{N}'(0)$	٠٠/١		
R44h	VCOM Control 2	W/R	1					VCN	[6:0] (101_10	10)			
R45h	VCOM Control 3	W/R	1						VD	V[4:0] (1_000	01)		
R46h	r1 Control (1)	W/R	1			G1 CP12(0)	G1 CP11(1)	G1 CP10(1)		G1 CP02(1)	G1 CP01(0)	G1 CP00(1)	
D47h	rt Control (2)	WIR	1			G1	G1	G1	40	G1	G1	G1	
R47h	r1 Control (2)	W/R	'			CN12(1)	CN11(0)	CN10(1)	111	CN02(0)	CN01(1)	CN00(1)	
R48h	r1 Control (3)	W/R	1			G1 NP12(1)	G1 NP11(0)	G1 NP10(0)	2/	G1 NP02(1)	G1 NP01(1)	G1 NP00(0)	
R49h	r1 Control (4)	W/R	1			G1	G1	G1	5).	G1	G1	G1	
174311	11 Collect (4)	WALL	<u>'</u>			NP32(0)	NP31(0)	NP30(1)		NP22(1)	NP21(1)	NP20(0)	
R4Ah	r1 Control (5)	W/R	1			G1 NP52(0)	G1 NP51(0)	G1 NP50(0)	٠.	G1 NP42(0)	G1 NP41(0)	G1 NP40(0)	
R4Bh	r1 Control (6)	W/R	1			G1	G1	G1		G1	G1	G1	
	11 0011001(0)	*****	-			NN12(1) G1	NN11(1) G1	NN10(1) G1	~(	NN02(1) G1	NN01(1) G1	NN00(1) G1	
R4Ch	r1 Control (7)	W/R	1			NN32(0)	NN31(0)	NN30(1)	·//	NN22(1)	NN21(1)	NN20(0	
R4Dh	r1 Control (8)	W/R	1			G1	G1 NNE1(0)	G1	$(\bigcirc)$	G1 NNA2(0)	G1	G1 NNAD/41	
						NN52(0)	NN51(0) G1	NN50(1)		NN42(0)	NN41(1)	NN40(1)	
R4Eh	r1 Control (9)	W/R	1	•		$\langle i \rangle$	CGMP1 (0)	G1 CGMP0(0)	G1 OP03(1)	G1 OP02(1)	G1 OP01(1)	G1 OP00(1)	
R4Fh	r1 Control (10)	W/R	1		G1 CGM2(0)	G1 CGM1(0)	G1_ CGMD (1)	G1 OP14(0)	G1 OP13(0)	G1 OP12(1)	G1 OP11(1)	G1 OP10(1)	
R50h	r1 Control (11)	W/R	1		(.)	) .	G1 CGMN1 (0)	G1 CGMN0 (0)	G1_ ON03(0)	G1_ ON02(1)	G1_ ON01(1)	G1_ OND0(1)	
R51h	r1 Control (12)	W/R	1	. /		G1_ GSEL(1)	7),	G1 ON14(1)	G1 ON13(1)	G1 ON12(1)	G1 ON11(1)	G1 ON10(0)	
R52h	OTP related1	WR	1	7	OTP_MASK7	OTP_MAS K5(0)	OTP_M ASK5(0)	OTP MA SK4(0)	OTP MA SK3(0)	OTP MA SK2(0)	OTP M ASK1(0)	OTP M ASKD(D)	
R53h	OTP related2	WR	1		OTP_INDEX 7(1)	OTP_INDE X6(1)	OTP_IN DEX5(1)	OTP IN DEX4(1)	OTP IN DEX3(1)	OTP IN DEX2(1)	OTP IN DEX1(1)	OTP IN DEX0(1)	
R54h	OTP related3	WR	1	107	OTP_LOAD_ DIŜABLE (0)	DOCLK_ DISABLE (0)	OTP_ POR (0)	OTP_PWE	OTP_NVAL ID (1)		VPP_SEL (0)	OTP_PRO G(II)	
R55h	Internal Use 1	W/R	A)							VD0	C_SEL[2:0] (	011)	
R56h	Internal Use 2	W/R	1	<i>&gt;</i> .	RPU	LSE[2:0] (000)		SRAM OPT(0)	SEN MODE(0)	SP	ULSE[2:0] (1	(00)	
R57h	Internal Use 3	WR	Y	10	1100			OP1(0)	MODE(U)		TEST MODE	TEST_ OE(0)	
R58h	Internal Use 4	W/R	1	1/	1.1			PROB[7:0]	(8'b0)		(0)	-(-)	<del></del>
R59h	Internal Use 5	W/R	1	. /				PTBA[15:8]					
R5Ah	Internal Use 6	W/R	1					PTBA[7:0]					
R58h	Internal Use 7	W/R	1					STBA[15:8]					
R5Ch	Internal Use 8	W/R	1				S	TBA[7:0] (10	00_0010)				
R5Dh	Internal Use 9	W/R	1				TSEL[2:0] (0				GAOE (0)	GAM (0)	
R5Eh	Internal Use 10	W/R	1		BIST CHKB1(0)	BIST CHKB0(0)	BIST ALL1(0)	BIST ALLO(0)	BIST V(0)	BIST H(0)	BIST OPT(0)	BIST EN(0)	
R5Fh	Internal Use 11	W/R	1		OTHER TOP	OI=(DU(O)		RRO_FLAG[		11(0)	O. 1(0)	214(0)	
R60h	Internal Use 12	W/R	1					-			PULO (0)	SRAM ADDR MUX(0)	
R61h	Internal Use 13	W/R	1					TSA(0)	ELE(0)	TDISP AREA(0)	TM(0)	TSC(0)	
R62h	Internal Use 14	W/R	1									TLADD (8)(D)	
R63h	Internal Use 15	W/R	1		TLADD[7:0] (8'b0)						<del>                                     </del>		
R64h	Internal Use 16	R	1		ID1[7:0] (8'00)								
R65h	Internal Use 17	W/R	1		1				D2[7:0] (8'b0)				
R66h	Internal Use 18	W/R	1					ID3[7:0] (					

Register No.	Register	W/R	R	Upper Code				Lower	Code				Comment
NO.	Ů		3	D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R67h	Driver ID	R	1		0	1	0	0	0	1	1	0	
R68h	Internal Use 20	W/R	1							ROM_TE	ST_ADDR[10		
R69h	Internal Use 21	W/R	1						-	ROM TEST(1)	ROM_ TEST CSB(1)	ROM_ TEST OEB(0)	
R70h	Logic Function register	W/R	1		OSC_SP EED(1)	GS(0)	SS(0)	TEMODE (0)	TEON(0)	C	SEL[2:0] (11	1)	
R72h	Internal Use 30	W/R	1								TRI[1:	0] (00)	
R73h	Internal Use 31	W/R	1			SDMYP0[7:0] (8'b1111_1111)							
R74h	Internal Use 32	W/R	1						SDM'	YB0[4:0](5'b1_	1111)		
R75h	Internal Use 33	W/R	1			SDMYP1[7:0](8'b1111_1111)							
R76h	Internal Use 34	W/R	1					SDMYB1[4:0](5'b1_1111)					
R77h	Internal Use 35	W/R	1					SDMYP2[7:0](8'b1111_1111)					
R78h	Internal Use 36	W/R	1					SDMYB2[4:0](5'b1_1111)					
R79h	Internal Use 37	W/R	1					SDMYP3[7:0](	811111_1111	1)			
R7Ah	Internal Use 38	W/R	1						SDM'	YB3[4:0](5'b1_	1111)		
R7Bh	Internal Use 39	W/R	1					SRAM FIX_EN (0)	6	10.		BIST LOAD(0)	
R7Ch	Internal Use 40	W/R	1						1./	v .		DBK(1)	
R7Dh	Internal Use 41	W/R	1					. //	S.V	В	RTH[2:0] (01	1)	
R7Eh	Internal Use 42	W/R	1						LE	D_PA[3:0] (11	01)		
R7Fh	Internal Use 43	W/R	1						LE	D_PB[3:0] (10	00)		
R80h	Internal Use 44	W/R	1						PWM_PE	RIOD[7:3] (5	b1_1111)		
R81h	Internal Use 45	W/R	1		PWM_F	PERIOD[2:0]	(3'b111)						
R82h	Internal Use 46	W/R	1				(22)		DUT	Y[4:0] (5'b1_1	1111)		
R83h	Internal Use 47	W/R	1				83	> ·	1:	9,	SFULL (0)	•	
R84h	Internal Use 48	W/R	1			. /	1.17			11.	IO_OPT[1	:0] (2'b10)	

## 6.0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Unit	Value
Power Supply Voltage (1)	$V_{DC}$	V	-0.3 to +4.6
Power Supply Voltage (1)	V <sub>CC1A</sub>	V	-0.3 to +4.6
Input Voltage	$V_{I}$	V	-0.3 to V <sub>CC1A</sub> +0.3

## 7.0 ELECTRICAL CHARACTERISTICS

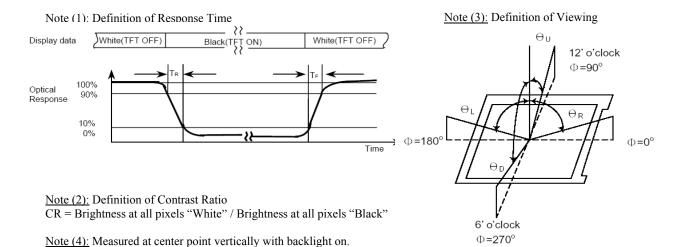
Item	Symbol	Min	Typ.	Max	Unit	Remarks
Digital Dawar valtaga	DVDC	2.5	2.8	3.3	V	
Digital Power voltage	AVDC	2.5	2.8	3.3	V	
Gate on voltage	$V_{ m GH}$	-	15	-	V	
Gate off voltage	$ m V_{GL}$	-	-8	-	V	
I/O Power supply	V <sub>CC1A</sub>	1.7	-	3.3	V	
Input high voltage	$V_{\mathrm{IH}}$	0.8*V <sub>CC1A</sub>	-	V <sub>CC1A</sub>	V	
Input low voltage	$V_{\rm IL1}$	GND	-	0.2*V <sub>CC1A</sub>	V	

## 8.0 BACKLIGHT SPECIFICATIONS

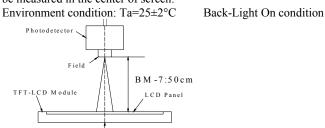
Item	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Forward voltage	Vf	12	12.8	13.2	V	If = 15  mA	
Forward Current	If	-	15	-	mA		
Reverse Voltage	Vr	-	-	5	V		
Reverse current	Ir	-	-	15	μΑ	Vr = 3.0V	
Chromaticity	X	0.283	-	0.330	-		
coordinates	Y	0.276	-	0.330	-		
Luminance (BLU only)	Lv	2800	3400	3700	cd/m <sup>2</sup>	If = 15  mA	
Uniformity	Δ	80	85	-	%	Min/max*100%	
Half-Brightness Life Time	50000 hours						

## **OPTICAL CHARACTERISTICS** (Ta=25°C)

No	Item		Symbol	Condition	Min.	Тур.	Max.	Unit	Note
1	Response	Rise	Tr	$\theta = \phi = 0_{\rm o}$	-	15	30	ms	(1)
	Time	Fall	Tf	$\theta = \phi = 0_{\rm o}$	-	35	50	ms	
2	Contrast Ratio		CR	$\theta = \phi = 0_{\rm o}$	150	250	-	-	(2)
3	Viewing Angle	,	Right	$\phi = 0_{\rm o}$	40	45		Deg	(3)
	$(CR \ge 10)$		Left	$\phi = 180^{\circ}$	40	45		Deg	
			Upper	$\phi = 90^{\circ}$	10	15		Deg	
			Lower	$\phi = 270^{\circ}$	30	35		Deg	
4	Color	Red	Rx	$\theta = \phi = 0_{\rm o}$	0.610	0.640	0.670	-	(4)
	Chromaticity		Ry		0.314	0.344	0.374	-	
	(CIE1931)	Green	Gx		0.268	0.398	0.328	-	
			Gy		0.553	0.583	0.613	-	
		Blue	Bx		0.102	0.132	0.162	-	
			By		0.107	0.137	0.167	-	
		White	Wx		0.282	0.312	0.342	-	
			Wy		0.319	0.349	0.379	-	
5	Luminance of		L		250	t.b.d.	-	Cd/m <sup>2</sup>	(5)
	white (Center								
	point of								
	LCM)								



Note(5): After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed .Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the back-light. This should be measured in the center of screen.



### 10.0 STANDARD SPECIFICATION FOR RELIABILITY

#### 10.1 **Standard specification of Reliability Test**

No	Test Item	Content of Test	<b>Test Condition</b>	Applicable Standard						
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80+/-3 °C 240 hrs							
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30+/-3 °C 240 hrs							
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70+/-3 °C 240 hrs							
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20+/-3 °C 240 hrs							
5	High temperature / Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40 °C, 90 %RH 120 hrs	MIL-202E- 103B JIS-C5023						
6	Temperature cycle	Endurance test applying the low and high temperature cycle.  -20°C \( \frac{25°C}{30min.} \) \( \frac{25°C}{5min.} \) \( \frac{70°C}{30min.} \)	-20°C / 70°C 10 cycles							
	Mechanical Test									
7	Drop Test	Endurance test applying the drop during transportation.	Packed, 100cm free fall (6 sides, 1 corner, 3edges)							

#### Remarks:

- For operation test, above specification is applicable when test pattern is changing during entire operation test.
   Inspections after reliability tests are performed when the display temperature resumes back to room temperature.
- 3) It is a normal characteristic that some display abnormality can be seen during reliability test. If the display abnormality can resume back to normal condition at room temperature within 24hours, there is no permanent destruction over the display. The display still possesses its functionality after reliability tests.

#### 10.2 Failure Judgment Criteria

After the reliability tests above, test sample shall be let return to room temperature and humidity for at least 4 hours before final tests are carried out.

Criterion Item	Failure Judgment Criteria	
Electrical characteristic	Electrical short and open.	
Mechanical characteristic	Out of mechanical specification	
Optical characteristic	Out of the Appearance Standard	

## 11.0 QUALITY ASSURANCE

### 11.1 Acceptable Quality Level (AQL)

Each lot should satisfy the quality level defined as follows:

- a) Inspection method: MIL-STD-105E Level II normal one time sampling
- b) AQL level

Category	AQL	Definition	
Major	0.25%	Functional defective as product	
Minor	1.00%	Satisfy all functions as product but not satisfy cosmetic standard	

#### 11.2 Cosmetic Screening Criteria

No	Defect	Judgment Criteria				
1	Spots/Dust /Bubble (Round type)	Size, d (mm) Acceptable quantity in active area  d < 0.15  Disregard		Minor		
2	Dust/Scratches/ Black streak (Line type)		Length, L (mm)  Disregard $L \le 1.0$ $L \le 2.0$ Disregard	Acceptable quantity in active area Disregard Disregard 3	Minor	
3	Allowable density	Above defects should be separated more than 5mm each other.			Minor	
4	Rainbow	Obvious unven color (rainbow) shall not be noticeable.				
5	Display condition	Dim display on the not acceptable.	Major			
6	No display or missing display	The patterns of dis missing display ar	Major			

#### 12.0 PRECAUTIONS FOR USING LCD MODULE

#### **Handing Precautions**

- The display panel is made of glass and polarizer. Do not subject it to mechanical shock by dropping or impact which may cause chipping especially on the edges.
- Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.). The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with Isopropyl alcohol or ethyl alcohol. Avoid using solvents like acetone (ketene), water, toluene, ethanol to clean the polarizer surface.
- Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion.
- Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- NC terminal should be open. Do not connect anything.
- If the logic circuit power is off, do not apply the input signals.
- Avoid contacting oil and fats.
- Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.
- Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

#### **Electro-Static Discharge Control**

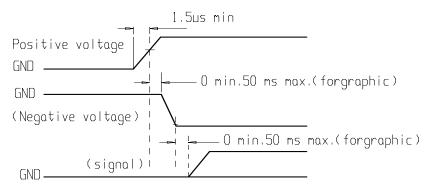
- Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.
- Be sure to ground the body when handling the LCD modules. Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions. To reduce the generation of static electricity, be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

#### **Precaution for soldering to the LCM**

- Observe the following when soldering lead wire, connector cable and etc. to the LCD module.
- Soldering iron temperature: 300 ~ 350°C.
- Soldering time:  $\leq 3$  sec.
- Solder: eutectic solder.
- Above is a recommended approach. Due to different solder composition and processing method, it is recommended that customer to study and fine tuning their soldering process parameters accordingly.
- If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

#### **Precautions for Operation**

- Viewing angle varies with the change of liquid crystal driving voltage (V<sub>O</sub>). Adjust V<sub>O</sub> to show the best contrast.
- Driving the LCD in the voltage above the limit shortens its lifetime.
- Response time is greatly delayed at temperature below the operating temperature range. However, it will recover when it returns to the specified temperature range.
- If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.
- When turning the power on, input each signal after the positive/negative voltage becomes stable.



#### **Storage**

- When storing LCDs as spares for some years, the following precautions are necessary.
- Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.
- Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.
- Environmental conditions:
  - Do not leave them for more than 168hrs. at 60°C.
  - Should not be left for more than 48hrs. at -20°C.

#### **Safety**

- It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

#### 13.0 LOT NUMBERING SYSTEM

#### 13.1 Definition of Lot Number

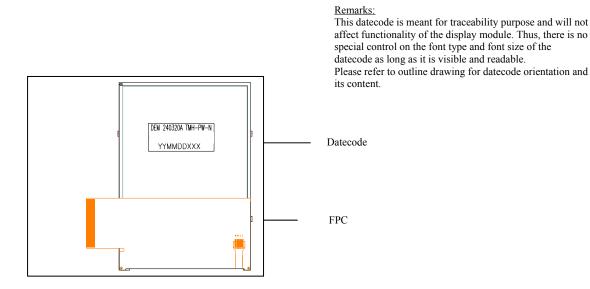
One lot means the delivery date and times to customer at one time.

## YYMMDD XXX

(1) Manufacturing date (COG bonding) (YY: Year, MM: Month, DD: Day)

(2) Serial number starts from A01, A02...., A99, B01, B02....

#### 13.2 Location of lot number



#### 14.0 ROHS COMPLIANT PRODUCT

#### Standard of specific chemical substance

1.	Cadmium and Cadmium Compounds	Less than 100ppm
2.	Hexavalent Chromium Compounds	Less than 1000ppm
3.	Lead and Lead Compounds	Less than 1000ppm
4.	Mercury and Mercury Compounds	Less than 1000ppm
5.	Polybrominated Biphenyls (PBBs)	Less than 1000ppm
6.	Polybrominated Diphenyl ethers (PBDEs)	Less than 1000ppm

#### 15.0 LIMITED WARRANTY

Please inspect the LCD modules within one month after your receipt. Unless agreed between DISPLAY and customer, DISPLAY will replace or repair any of its LCD modules, which are found to be functionally defective when inspected in accordance with DISPLAY LCD/LCM acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to DISPLAY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DISPLAY limited to repair and/or replacement on the terms set forth above. DISPLAY will not be responsible for any subsequent or consequential events.