Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 128064G - Y

Product Specification ***Version : 01***

28.05.2007

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2007/05/28	SPEC.

C O N T E N T S

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128×64	dots
Module dimension (L*W*H)	76.65*52.7*8.5(MAX)	mm
View area	60.0*32.5	mm
Active area	55.01*27.49	mm
Dot size	0.40(W)×0.40(H)	mm
Dot pitch	0.43(W)×0.43 (H)	mm

(2) Controller IC: SSD1303 Controller

(3) Temperature Range

Operating	-40 ~ +85℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+85	℃
Storage Temperature	TST	-40	—	+85	℃
Input Voltage	VI	—	—	VDD	V
Operating lift time			66000(*)		Hrs

*:60cd/m^2 light on

4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	2.4	2.5	3.5	V
Input High Vol	V_{IH}	—	0.7V_{DD}	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	0.3V_{DD}	V
Output High Vol	V_{OH}	—	2.4	—	—	V
Output Low Vol.	V_{OL}	—	—	—	0.4	V
Supply Current	I_{DD}	—	—	120.0	—	mA

5. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) θ	CR≧20	85		85	deg
	(H) φ	CR≧20	85		85	deg
Contrast Ratio	CR	—		100		—
Response Time 25℃	T rise	—		40		ms
	T fall	—		40		ms

6. Interface Pin Function

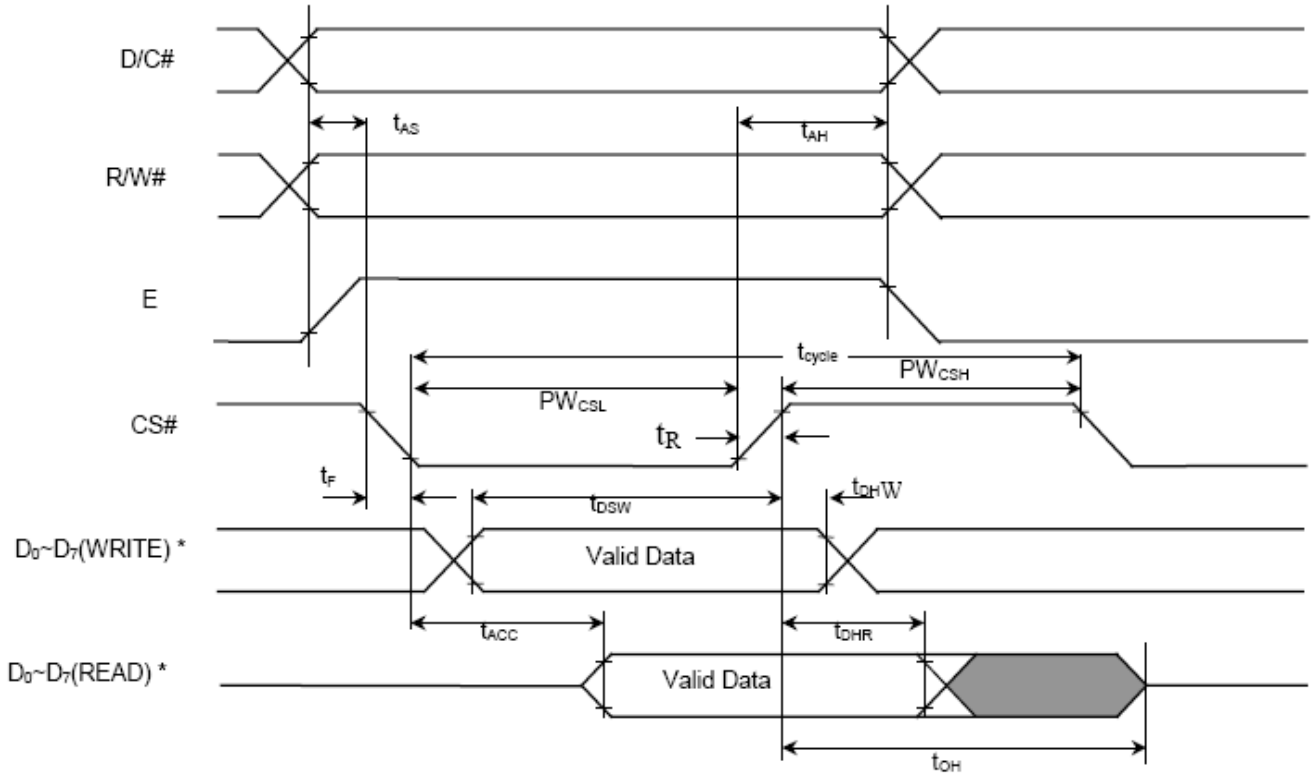
Pin No.	Symbol	Level	Description
1	Vdd	3.3V	Supply voltage for logic
2	Vss	0V	Ground
3	NC	—	No connection
4	DB0	H/L	Data bus line
5	DB1	H/L	Data bus line
6	DB2	H/L	Data bus line
7	DB3	H/L	Data bus line
8	DB4	H/L	Data bus line
9	DB5	H/L	Data bus line
10	DB6	H/L	Data bus line
11	DB7	H/L	Data bus line
12	CS	H/L	Chip select pin
13	NC	—	No connection
14	/RES	H/L	Hardware Reset pin
15	WR	H/L	8080: data write enable pin 6800: Read/Write select pin
16	RS	H/L	H: Data; L: Command.
17	RD	H/L	8080: data read enable pin 6800: Read/Write enable pin
18	NC	—	No connection
19	DISP	L	L:LCM display off
20	NC	—	No connection

※80 Series Interface is Default
(6800 series MPU interface is option)
(SPI interface is option)

7. Timing Characteristics

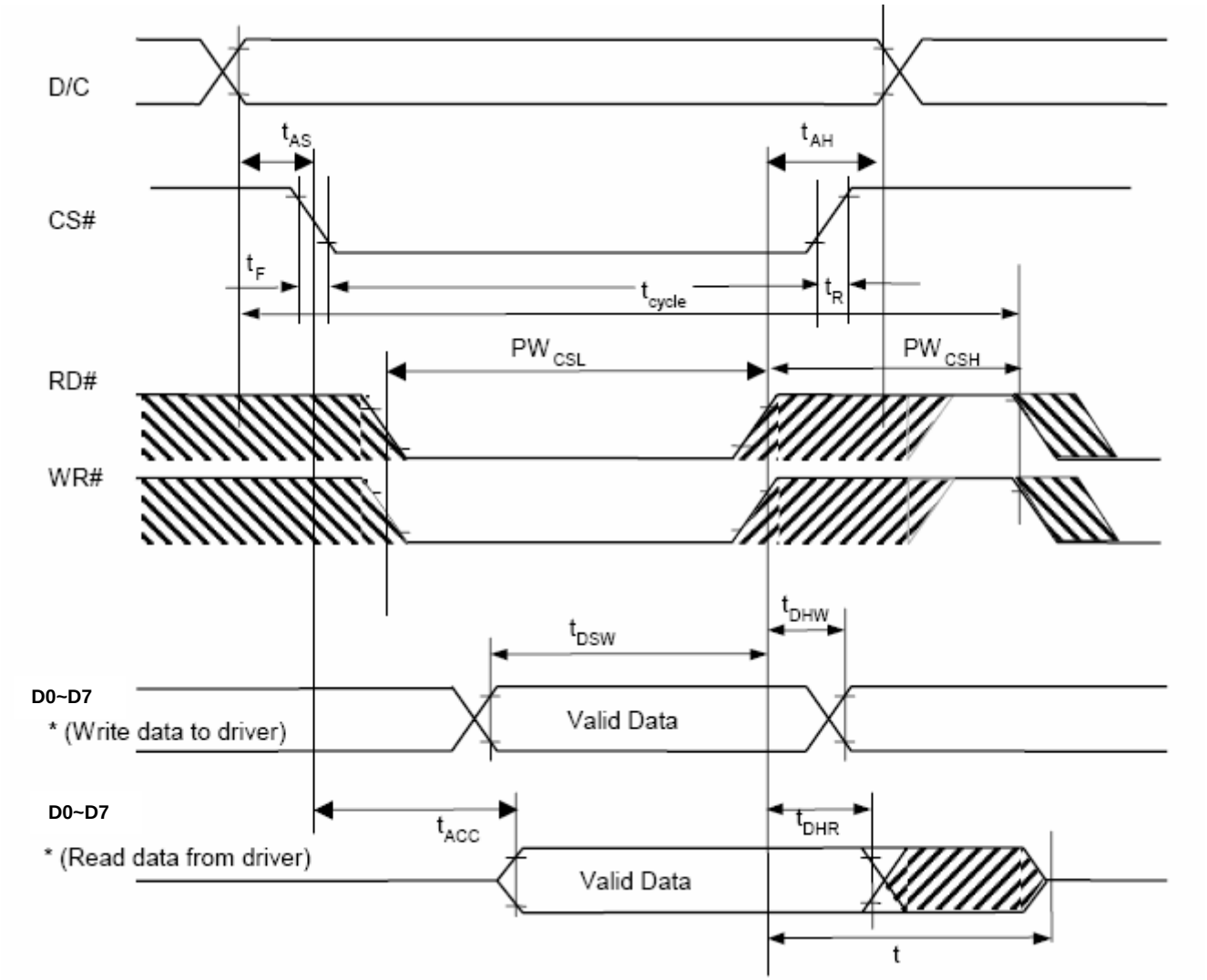
7-1.6800 MPU Interfac

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock Cycle Time	300	-	-	ns
tAS	Address Setup Time	0	-	-	ns
tAH	Address Hold Time	0	-	-	ns
tDSW	Write Data Setup Time	40	-	-	ns
tDHW	Write Data Hold Time	15	-	-	ns
tDHR	Read Data Hold Time	20	-	-	ns
tOH	Output Disable Time	-	-	70	ns
tACC	Access Time	-	-	140	ns
PWCSL	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PWCSH	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
tR	Rise Time	-	-	15	ns
tF	Fall Time	-	-	15	ns



7-2.8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock Cycle Time	300	–	–	ns
tAS	Address Setup Time	0	–	–	ns
tAH	Address Hold Time	0	–	–	ns
tDSW	Write Data Setup Time	40	–	–	ns
tDHW	Write Data Hold Time	15	–	–	ns
tDHR	Read Data Hold Time	20	–	–	ns
tOH	Output Disable Time	–	–	70	ns
tACC	Access Time	–	–	140	ns
PWCSL	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	–	–	ns
PWCSH	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	–	–	ns
tR	Rise Time	–	–	15	ns
tF	Fall Time	–	–	15	ns



8. Display Control Instruction

(**D/C** = 0, **R/W** (**WR**) = 0, E(**RD**) = 1) unless specific setting is stated
Single byte command (D/C = 0), Multiple byte command (D/C = 0 for first byte, D/C = 1 for other bytes)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X3	X2	X1	X0	Set Lower Column Address **	Set the lower nibble of the column address register using X3X2X1X0 as data bits. The initial display line register is reset to 0000b after POR.
0	10~1F	0	0	0	1	X3	X2	X1	X0	Set Higher Column Address **	Set the higher nibble of the column address register using X3X2X1X0 as data bits. The initial display line register is reset to 0000b after POR.
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[2:0] Set the number of column scroll per step
0	A[2:0]	*	*	*	*	*	A2	A1	A0		Valid value: 001b, 010b, 011b, 100b
0	B[2:0]	*	*	*	*	*	B2	B1	B0		B[2:0] Define start page address
0	C[1:0]	*	*	*	*	*	*	C1	C0		C[1:0] Set time interval between each scroll step in terms of frame frequency
0	D[2:0]	*	*	*	*	*	D2	D1	D0		00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40-7F	0	1	X5	X4	X3	X2	X1	X0	Set Display Start Line	Set display TAM display start line register from 0-63 using X5X3X2X1X0. Display start line register is reset to 000000 during POR
0 0	81 A[7:0]	1 A7	0 A6	0 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 80h)
0	82	1	0	0	0	0	0	1	0	Brightness for color banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (POR = 80h)
A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0			
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT) for area colour	Set current drive pulse width of Bank 0, Colour A, B and C.
0	X[5:0]	*	*	X5	X4	X3	X2	X1	X0		Bank 0: X[5:0] = 0… 63; for pulse width set to 1 ~ 64 clocks (POR = 110001b)
0	A[5:0]	*	*	A5	A4	A3	A2	A1	A0		Colour A: A[5:0] same as above (POR = 111111b)
0	B[5:0]	*	*	B5	B4	B3	B2	B1	B0		Colour B: B[5:0] same as above (POR = 111111b)
0	C[5:0]	*	*	C5	C4	C3	C2	C1	C0		Colour C: C[5:0] same as above (POR = 111111b) Note: colour D pulse width is fixed at 64 clocks pulse .

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank colour of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 1
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 2
0	B[7:0]	B7	B6	B5	B4	B3	B2	B1	B0		:
0	C[7:0]	C7	C6	C5	C4	C3	C2	C1	C0		:
0	D[7:0]	D7	D6	D5	D4	D3	D2	D1	D0		D[7:6]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank colour of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 17
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 18
0	B[7:0]	B7	B6	B5	B4	B3	B2	B1	B0		:
0	C[7:0]	C7	C6	C5	C4	C3	C2	C1	C0		:
0	D[7:0]	D7	D6	D5	D4	D3	D2	D1	D0		D[7:6]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 32
0	A0~ A1	1	0	1	0	0	0	0	X0	Set Segment Re-map **	X0=0: column address 0 is mapped to SEG0 (POR) X0=1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X0	Set Entire Display ON/OFF **	X0=0: normal display (POR) X0=1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X0	Set Normal/Inverse Display **	X0=0: normal display (POR) X0=1: inverse display
0 0	A8 A[5:0]	1 *	0 *	1 A5	0 A4	1 A3	0 A2	0 A1	0 A0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, POR= 64MUX
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0 0	AD	1 1	0 0	1 0	0 0	1 1	1 0	0 1	1 X0	Set DC-DC on/off	X0 : 1 DC-DC will be turned on when display on (POR) 0 DC-DC is disable
0	AE~AF	1	0	1	0	1	1	1	X0	Set Display ON/OFF **	X0=0: turns OFF OLED panel (POR) X0=1: turns ON OLED panel
0	B0~BF	1	0	1	1	X3	X2	X1	X0	Set Page Address **	Set GDDRAM Page Address (0~7) for read/write using X3X2X1X0
0	C0/C8	1	1	0	0	X3	*	*	*	Set COM Output Scan Direction **	X3=0: normal mode (POR) Scan from COM 0 to COM [N –1] X3=1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X0	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	D3 A[5:0]	1 *	1 *	0 A5	1 A4	0 A3	0 A2	1 A1	1 A0	Set Display Offset **	Set vertical scroll by COM from 0-63. The value is reset to 00H after POR.
0 0	D5 A[7:0]	1 A7	1 A6	0 A5	1 A4	0 A3	1 A2	0 A1	1 A0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] Define the divide ratio of the display clocks (DCLK): Divide ratio= A[3:0] + 1, POR is 0000b (divide ratio = 1) A[7:4] Set the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. POR is 0111b
0 0	D8	1 0	1 0	0 X5	1 X4	1 0	0 X2	0 0	0 X0	Set area colour mode on/off & low power display mode	X5X4= 00 (POR) : mono mode X5X4= 11 Area Colour enable X2=0 and X0=0: Normal (POR) power mode X2=1 and X0=1: Set low power save mode
0 0	D9 A[7:0]	1 A7	1 A6	0 A5	1 A4	1 A3	0 A2	0 A1	1 A0	Set Pre-charge period**	A[3:0] Phase 1 period of up to 15 dclk clocks [POR=2h]; 0 is invalid entry A[7:4] Phase 2 period of up to 15 dclk clocks [POR=2h]; 0 is invalid entry
0 0	DA	1 0	1 0	0 0	1 X4	1 0	0 0	1 1	0 0	Set COM pins hardware configuration	X4=0, Sequential COM pin configuration (i.e. COM31, 30, 29….0 ; SEG0-132; COM31,32….62,63) X4=1(POR), Alternative COM pin configuration (i.e. COM62,60,58,…2,0; SEG0-132; COM1,3,5…61,63)
0 0	DB A[6:0]	1 *	1 A6	0 A5	1 A4	1 A3	0 A2	1 A1	1 A0	Set VCOM Deselect Level	A[6:0] 0000000 low VCOM deselect level (~ 0.43 Vref) 0110101 normal VCOM deselect level (~ 0.77*Vref (POR)) 1111111 high VCOM deselect level (equal Vref)
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

Note: Remark "*" stands for "Don't Care"

9. Appendix (Drawing)

PIN	Symbol
1	VDD
2	VSS
3	NC
4	DB0
5	DB1
6	DB2
7	DB3
8	DB4
9	DB5
10	DB6
11	DB7
12	CS
13	NC
14	/RES
15	R/W
16	D/C
17	E
18	NC
19	DISP
20	NC