Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 128064H - Y

Product Specification ***Version : 5***

26.09.2013

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2009/07/03	SPEC.
02	UPDATE Quality Assurance、Reliability ADD Precautions for Handling、Precautions for Electrical、Precautions for Storage	2012/08/17	SPEC
03	Modify Cover page	2012/10/17	Page1
04	Modify 10.3 Warranty Policy	2013/5/9	Page17
05	Modify Drawing	2013/09/26	Page 9

C O N T E N T S

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128x64	dots
Module dimension (L*W*H)	89.7*47.2*5.4(MAX)	mm
View area	57.01*29.4	mm
Active area	55.01*27.49	mm
Dot size	0.40(W)x0.40(H)	mm
Dot pitch	0.43(W)x0.43 (H)	mm

(2) Controller IC: SSD1303 Controller

(3) Temperature Range

Operating	-40 ~ +85℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature	TOP		-40	—	+85	℃
Storage Temperature	TST		-40	—	+85	℃
Input Voltage	VI		—	—	VDD	V
Operating lift time		100cd/m², 50% checkerboard	40000(1)			Hrs
Operating lift time		80cd/m², 50% checkerboard	50000(2)			Hrs
Operating lift time		60cd/m², 50% checkerboard	66000(3)			Hrs

Note:(A) Under VCC = 13V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m² :

- Contrast setting : 0XC5- Frame rate : 105Hz- Duty setting : 1/64

(2) Setting of 80 cd/m² :

- Contrast setting : 0x8F- Frame rate : 105Hz- Duty setting : 1/64

(3) Setting of 60 cd/m² :

- Contrast setting : 0x4C- Frame rate : 105Hz- Duty setting : 1/64

4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})	V_{DD}-V_{SS}	–	2.4	2.7	3.5	V
Supply Voltage (V_{cc})	V_{cc}-V_{SS}		12.5	13	13.5	V
Input High Vol	V_{IH}	–	0.8V_{DD}	–	V_{DD}	V
Input Low Vol	V_{IL}	–	0	–	0.2V_{DD}	V
Output High Vol	V_{OH}	–	0.9V_{DD}	–	–	V
Output Low Vol.	V_{OL}	–	–	–	0.1V_{DD}	V
Supply Current (with positive voltage)	I_{DD}	–	–	60	–	mA

5. Optical Characteristics

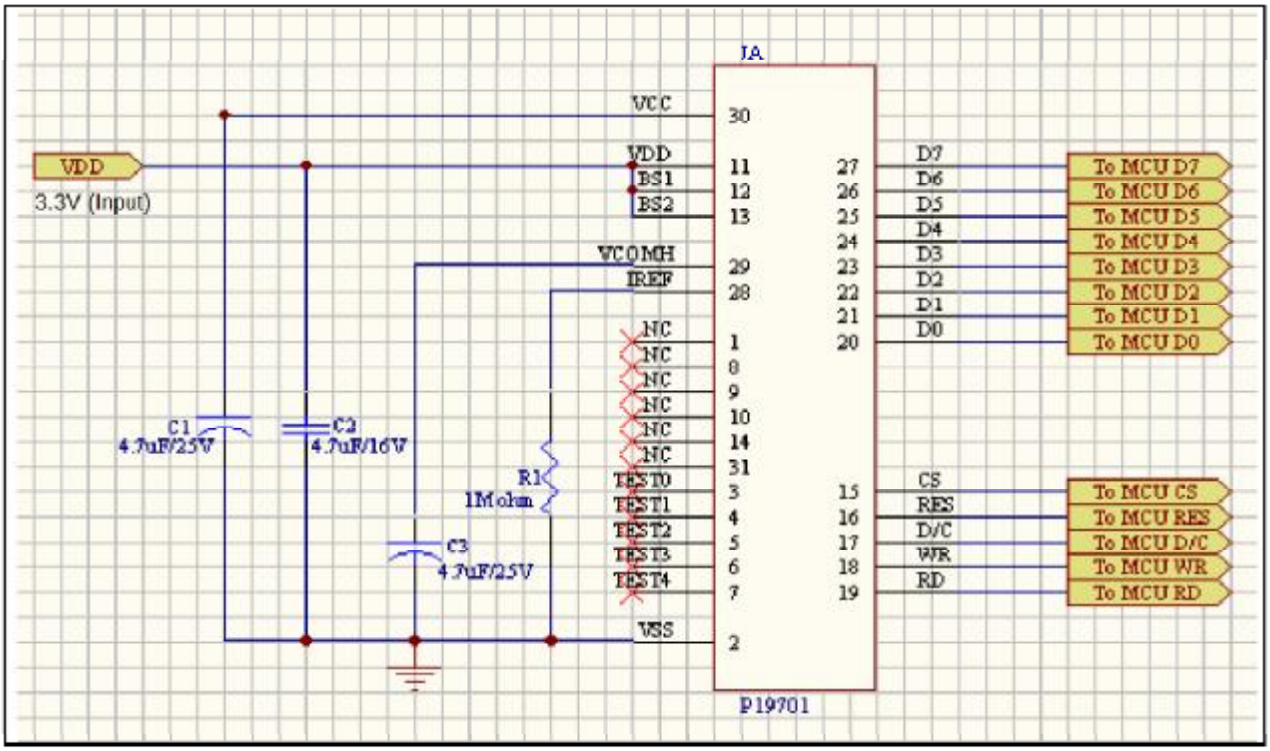
Item	Min.	Typ.	Max.	Unit
View Angle	160	–	–	deg
Dark Room contrast	2000:1	–	–	–
Response Time	–	10	–	us

6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	NC	–	No connection
2	VCC	–	Positive voltage power supply
3	VCOMH	–	The Com voltage reference input pin.a capacitor should be connected between this pin and Vss.
4	IREF	–	The Current voltage reference input pin.a resistor should be connected between this pin and Vss.
5	DB7	H/L	Data bus line
6	DB6	H/L	Data bus line
7	DB5	H/L	Data bus line
8	DB4	H/L	Data bus line
9	DB3	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB1	H/L	Data bus line
12	DB0	H/L	Data bus line
13	RD(E)	H/L	80: read signal , 68: enable signal
14	WR(R/W)	H/L	80: write signal 68:R/W signal
15	D/C	H/L	This is data/command control pin , H: Data input ,L: Command input .
16	RES	H/L	Hardware reset pin
17	CS	H/L	This is chip select control pin
18	NC	–	No connection
19	BS2	H/L	MCU interface selection input
20	BS1	H/L	MCU interface selection input
21	VDD	–	Voltage power supply for logic
22	NC	–	No connection
23	NC	–	No connection
24	NC	–	No connection
25	NC		No connection
26	NC		No connection
27	NC		No connection
28	NC		No connection
29	VSS		This is ground pin
30	NC		No connection

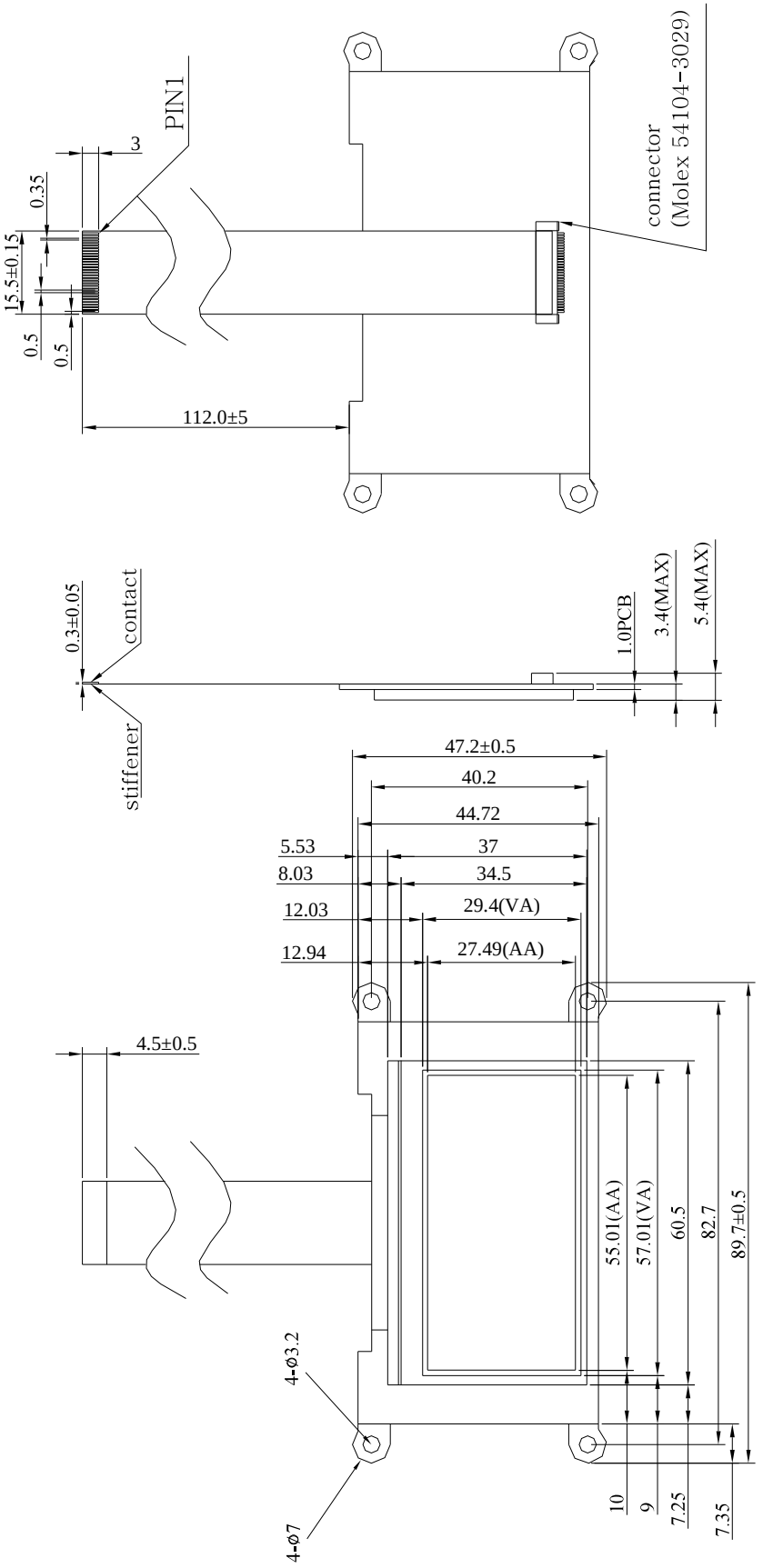
7. APPLICATION CIRCUIT

7.1 Built-In Positive Voltage Circuit



Recommended components
R1 : 1M ohm (0603),1%.
C1 : 4.7uF (Tantalum Type) / 25V, C2 : 4.7uF (0805) / 16V ,
C3 : 4.7uF (Tantalum Type) / 25V.
This circuit is designed for 8080 8-bits interface.

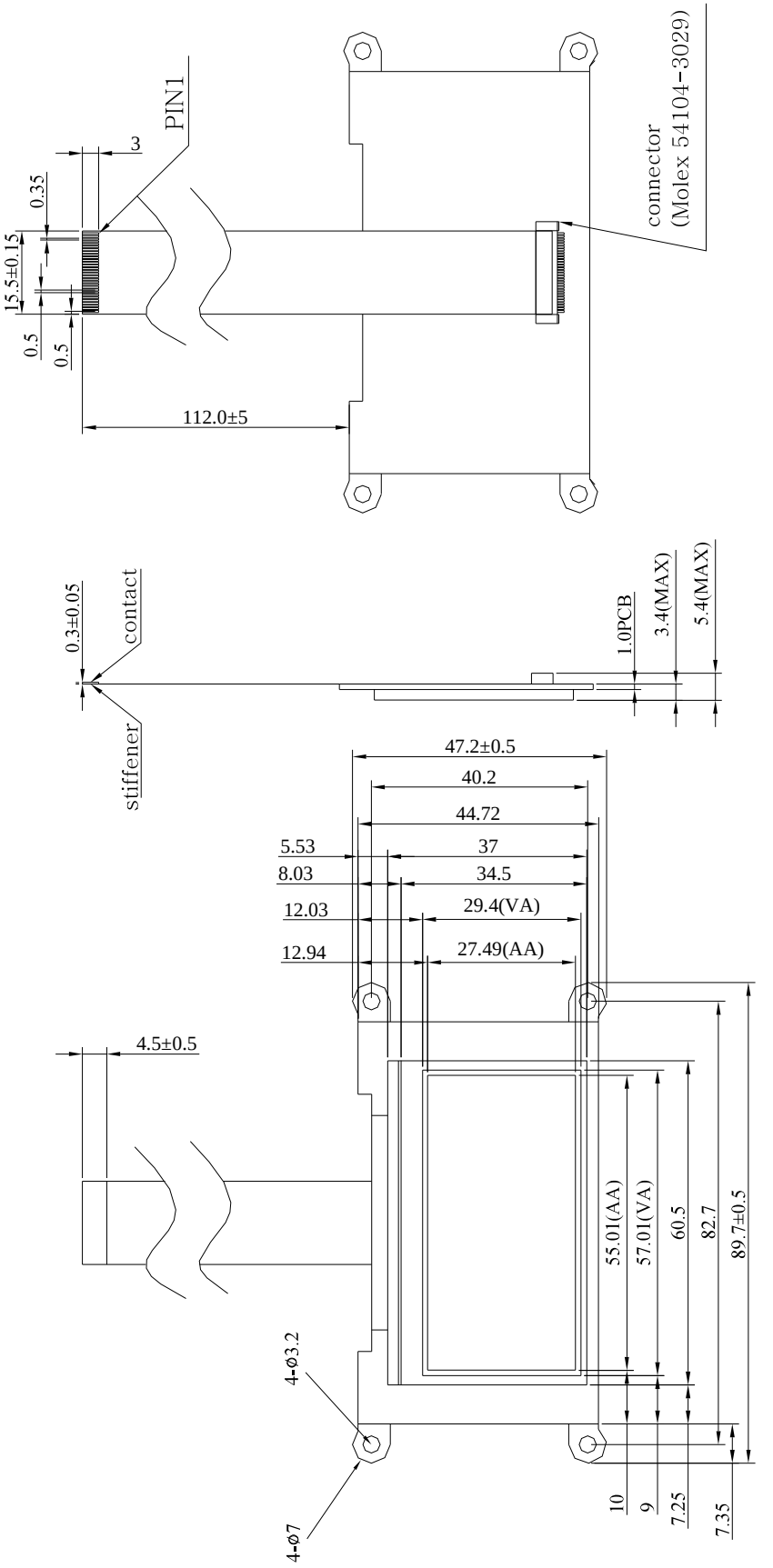
8. Drawing



PIN NO	SYMBOL	PIN NO	SYMBOL	PIN NO	SYMBOL
1	NC	11	D1	21	VDD
2	VCC	12	D0	22	NC
3	VCOMH	13	E/RD#	23	NC
4	IREF	14	R/W#	24	NC
5	D7	15	D/C#	25	NC
6	D6	16	RES#	26	NC
7	D5	17	CS#	27	NC
8	D4	18	NC	28	NC
9	D3	19	BS2	29	VSS
10	D2	20	BS1	30	NC

The non-specified tolerance of dimension is ±0.3 mm .

8. Drawing

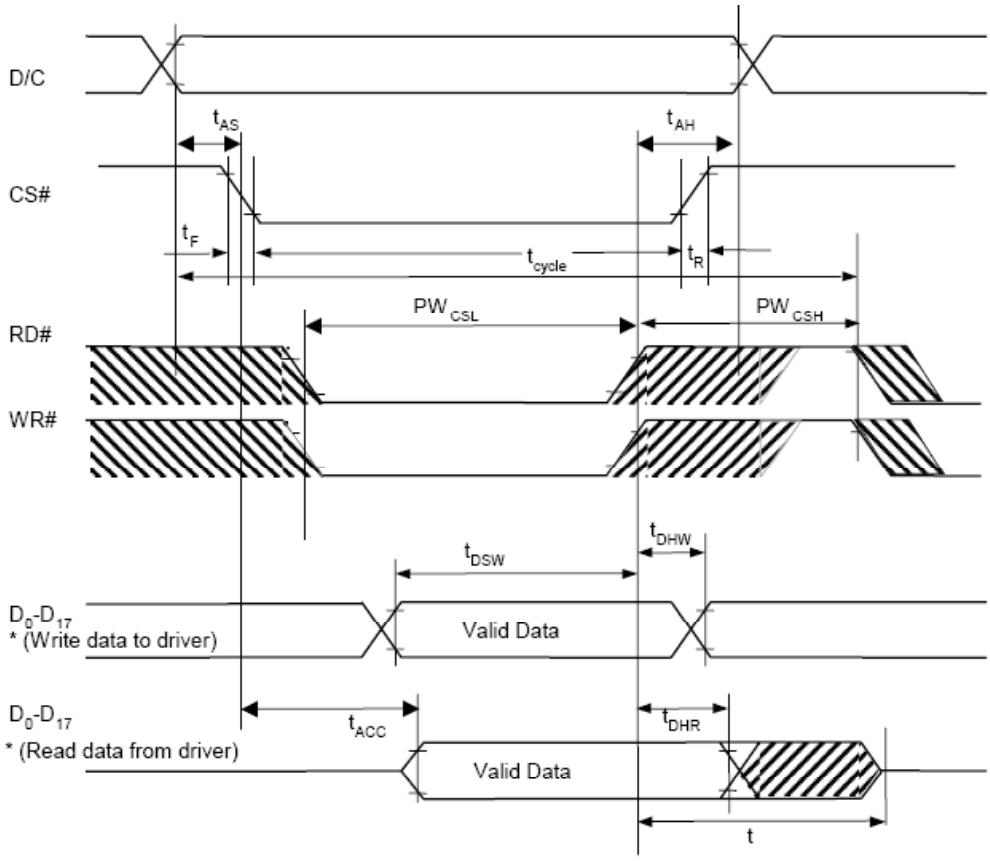


PIN NO	SYMBOL	PIN NO	SYMBOL	PIN NO	SYMBOL
1	NC	11	D1	21	VDD
2	VCC	12	D0	22	NC
3	VCOMH	13	E/RD#	23	NC
4	IREF	14	R/W#	24	NC
5	D7	15	D/C#	25	NC
6	D6	16	RES#	26	NC
7	D5	17	CS#	27	NC
8	D4	18	NC	28	NC
9	D3	19	BS2	29	VSS
10	D2	20	BS1	30	NC

The non-specified tolerance of dimension is ±0.3 mm .

8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock Cycle Time	300	-	-	ns
tAS	Address Setup Time	0	-	-	ns
tAH	Address Hold Time	0	-	-	ns
tDSW	Write Data Setup Time	40	-	-	ns
tDHW	Write Data Hold Time	15	-	-	ns
tDHR	Read Data Hold Time	20	-	-	ns
tOH	Output Disable Time	-	-	70	ns
tACC	Access Time	-	-	140	ns
PWCSL	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PWCSH	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
tR	Rise Time	-	-	15	ns
tF	Fall Time	-	-	15	ns



9.2 Display Control Instruction

(**D/C** = 0, **R/W** (**WR**) = 0, E(**RD**) = 1) unless specific setting is stated
Single byte command (D/C = 0), Multiple byte command (D/C = 0 for first byte, D/C = 1 for other bytes)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X3	X2	X1	X0	Set Lower Column Address **	Set the lower nibble of the column address register using X3X2X1X0 as data bits. The initial display line register is reset to 0000b after POR.
0	10~1F	0	0	0	1	X3	X2	X1	X0	Set Higher Column Address **	Set the higher nibble of the column address register using X3X2X1X0 as data bits. The initial display line register is reset to 0000b after POR.
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[2:0] Set the number of column scroll per step
0	A[2:0]	*	*	*	*	*	A2	A1	A0		Valid value: 001b, 010b, 011b, 100b
0	B[2:0]	*	*	*	*	*	B2	B1	B0		B[2:0] Define start page address
0	C[1:0]	*	*	*	*	*	*	C1	C0		C[1:0] Set time interval between each scroll step in terms of frame frequency
0	D[2:0]	*	*	*	*	*	D2	D1	D0		00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40-7F	0	1	X5	X4	X3	X2	X1	X0	Set Display Start Line	Set display TAM display start line register from 0-63 using X5X3X2X1X0. Display start line register is reset to 000000 during POR
0 0	81 A[7:0]	1 A7	0 A6	0 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 80h)
0	82	1	0	0	0	0	0	1	0	Brightness for color banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (POR = 80h)
A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0			
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT) for area colour	Set current drive pulse width of Bank 0, Colour A, B and C.
0	X[5:0]	*	*	X5	X4	X3	X2	X1	X0		Bank 0: X[5:0] = 0… 63; for pulse width set to 1 ~ 64 clocks (POR = 110001b)
0	A[5:0]	*	*	A5	A4	A3	A2	A1	A0		Colour A: A[5:0] same as above (POR = 111111b)
0	B[5:0]	*	*	B5	B4	B3	B2	B1	B0		Colour B: B[5:0] same as above (POR = 111111b)
0	C[5:0]	*	*	C5	C4	C3	C2	C1	C0		Colour C: C[5:0] same as above (POR = 111111b) Note: colour D pulse width is fixed at 64 clocks pulse .

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank colour of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 1
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 2
0	B[7:0]	B7	B6	B5	B4	B3	B2	B1	B0		:
0	C[7:0]	C7	C6	C5	C4	C3	C2	C1	C0		:
0	D[7:0]	D7	D6	D5	D4	D3	D2	D1	D0		D[7:6]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank colour of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 17
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		A[3:2] : 00, 01, 10, or 11 for Colour = A, B, C or D of bank 18
0	B[7:0]	B7	B6	B5	B4	B3	B2	B1	B0		:
0	C[7:0]	C7	C6	C5	C4	C3	C2	C1	C0		:
0	D[7:0]	D7	D6	D5	D4	D3	D2	D1	D0		D[7:6]: 00, 01, 10, or 11 for Colour = A, B, C or D of bank 32
0	A0~ A1	1	0	1	0	0	0	0	X0	Set Segment Re-map **	X0=0: column address 0 is mapped to SEG0 (POR) X0=1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X0	Set Entire Display ON/OFF **	X0=0: normal display (POR) X0=1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X0	Set Normal/Inverse Display **	X0=0: normal display (POR) X0=1: inverse display
0 0	A8 A[5:0]	1 *	0 *	1 A5	0 A4	1 A3	0 A2	0 A1	0 A0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, POR= 64MUX
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0 0	AD	1 1	0 0	1 0	0 0	1 1	1 0	0 1	1 X0	Set DC-DC on/off	X0 : 1 DC-DC will be turned on when (POR) display on 0 DC-DC is disable
0	AE~AF	1	0	1	0	1	1	1	X0	Set Display ON/OFF **	X0=0: turns OFF OLED panel (POR) X0=1: turns ON OLED panel
0	B0~BF	1	0	1	1	X3	X2	X1	X0	Set Page Address **	Set GDDRAM Page Address (0~7) for read/write using X3X2X1X0
0	C0/C8	1	1	0	0	X3	*	*	*	Set COM Output Scan Direction **	X3=0: normal mode (POR) Scan from COM 0 to COM [N –1] X3=1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X0	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	D3 A[5:0]	1 *	1 *	0 A5	1 A4	0 A3	0 A2	1 A1	1 A0	Set Display Offset **	Set vertical scroll by COM from 0-63. The value is reset to 00H after POR.
0 0	D5 A[7:0]	1 A7	1 A6	0 A5	1 A4	0 A3	1 A2	0 A1	1 A0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] Define the divide ratio of the display clocks (DCLK): Divide ratio= A[3:0] + 1, POR is 0000b (divide ratio = 1) A[7:4] Set the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. POR is 0111b
0 0	D8	1 0	1 0	0 X5	1 X4	1 0	0 X2	0 0	0 X0	Set area colour mode on/off & low power display mode	X5X4= 00 (POR) : mono mode X5X4= 11 Area Colour enable X2=0 and X0=0: Normal (POR) power mode X2=1 and X0=1: Set low power save mode
0 0	D9 A[7:0]	1 A7	1 A6	0 A5	1 A4	1 A3	0 A2	0 A1	1 A0	Set Pre-charge period**	A[3:0] Phase 1 period of up to 15 dclk clocks [POR=2h]; 0 is invalid entry A[7:4] Phase 2 period of up to 15 dclk clocks [POR=2h]; 0 is invalid entry
0 0	DA	1 0	1 0	0 0	1 X4	1 0	0 0	1 1	0 0	Set COM pins hardware configuration	X4=0, Sequential COM pin configuration (i.e. COM31, 30, 29….0 ; SEG0-132; COM31,32….62,63) X4=1(POR), Alternative COM pin configuration (i.e. COM62,60,58,…2,0; SEG0-132; COM1,3,5…61,63)
0 0	DB A[6:0]	1 *	1 A6	0 A5	1 A4	1 A3	0 A2	1 A1	1 A0	Set VCOM Deselect Level	A[6:0] 0000000 low VCOM deselect level (~ 0.43 Vref) 0110101 normal VCOM deselect level (~ 0.77*Vref (POR)) 1111111 high VCOM deselect level (equal Vref)
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

Note: Remark "*" stands for "Don't Care"

10 Quality Assurance

10.1 Inspection conditions

1. The inspection and meaurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5°C
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector≧30cm

10.2 Inspection Parameters

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm)
W</th><th>Length (mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜ W≦0.05</td><td>L≦3</td><td>3</td></tr>
<tr><td>0.05＜ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ≦0.2</td><td>Ignore</td></tr>
<tr><td>0.2＜Φ≦0.5</td><td>2</td></tr>
<tr><td>0.5＜Φ</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、
Lighting spot、
Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.15</td><td>2</td></tr>
<tr><td>0.15＜ D ≦0.2</td><td>1</td></tr>
<tr><td>0.2 ＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

10.3 WARRANTY POLICY

Supplier will provide one-year warranty for the products only if under specification operating conditions.

If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis. Supplier would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 40K hours.

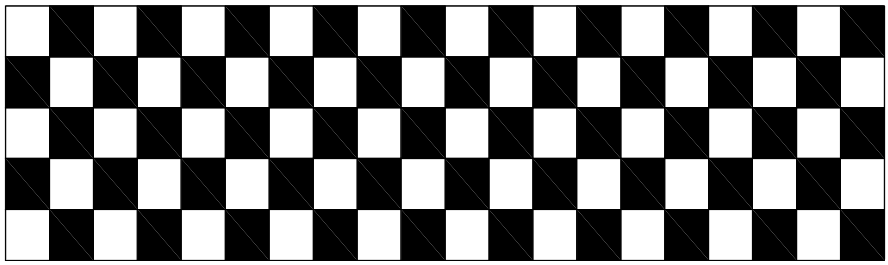
10.4.2 Test Condition:

10.4.2.1 Supply Voltage: Vcc=13V

10.4.2.2 Luminance: 100cd/m2

10.4.2.3 Operation temperature and humidity: 25 ℃ and 50%RH

10.4.2.4 Run-Patterns:



10.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.

11.Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption : within ±50% of initial value.

Reliability Test

Supplier only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.

12.Precautions for Handling

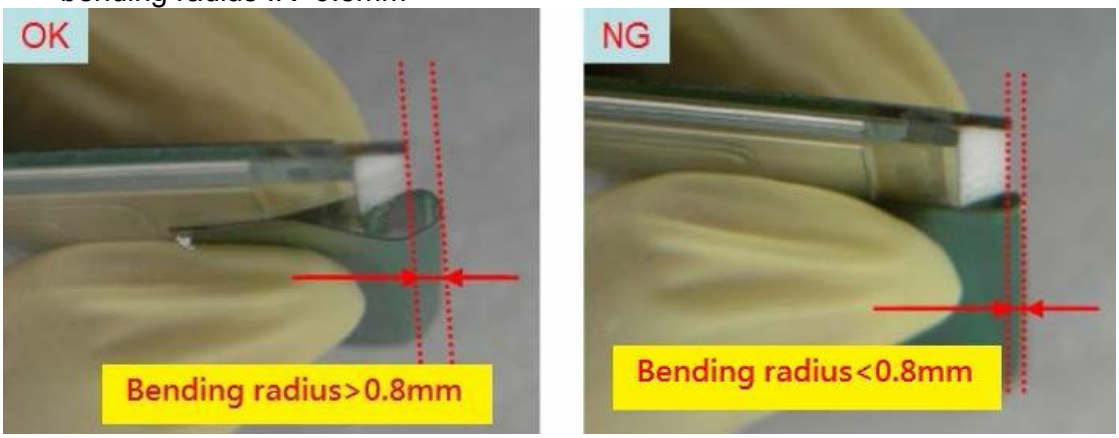
12.1 When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

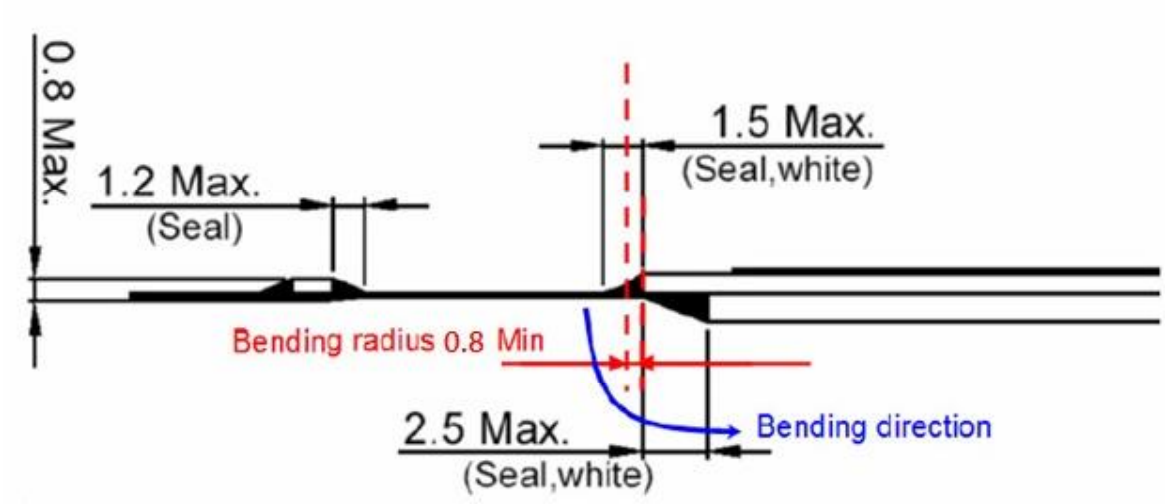
12.2 The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a height.

12.3 The OLED module is an electronic component and is subject to damage caused by Electro Static

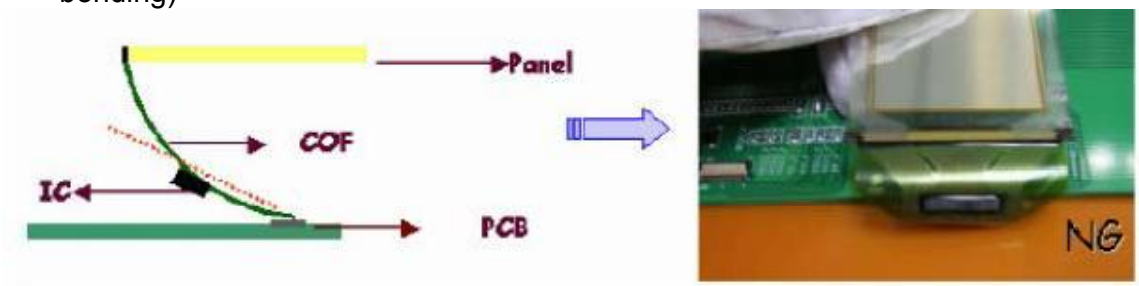
Discharge (ESD) and hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. (See the photos below).

12.4 Please do not bend the film near the substrate glass.(this could cause film peeling and COF damage) and the peeling strength about 600g/cm, the bending <20times and the bending radius :R>0.8mm

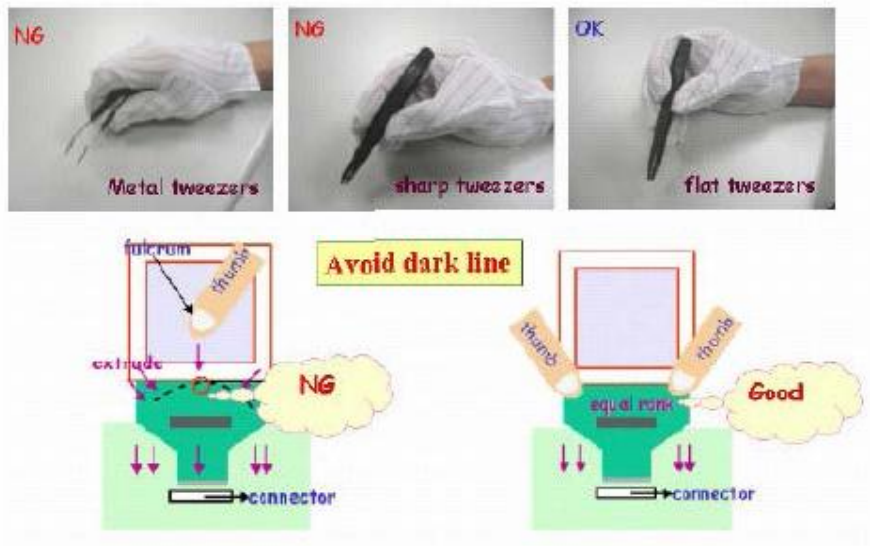




12.5 Avoid bending the film at IC bonding area.(>1.5mm)(this could damage the ILB bonding)



12.6 Use both thumbs to insert COF into the connector when assembling the panel. See the photo on the far right below for correct insertion of the film into the connector (one-handed insertion exerts uneven force on the film and could cause its breakage, photo on the left)



12.7 Do not wipe the pin of film with the dry or hard materials that will damage the surface. When cleaning the display surface, use soft cloth solvent and wipe gently (Recommend solvent: IPA, alcohol), and do not wipe the display with dry or hard materials that will damage the polarizer surface and do not use the solvent like: Water, Acetone, Aromatic

13. Precautions for Electrical

13.1. Design using the settings in the specification

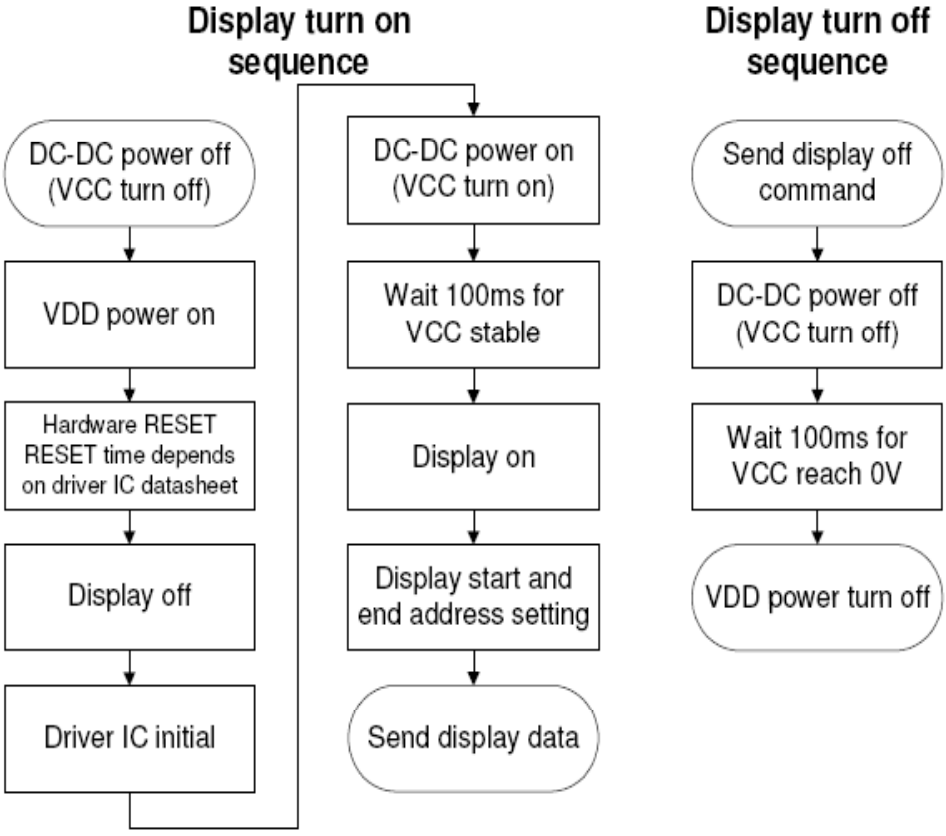
It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2. Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel malfunctioning.



13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode.

The power consumption is almost in direct proportion to the brightness of the panel, and also in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

13.5.1 Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.

13.5.2 Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays

13.5.3 If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns

14. Precautions for Storage

Although the storage conditions and guarantee period are indicated in the specification, it is advisable to store the packed cartons or packages at 23℃±5℃,55%±10%RH, Do not store the OLED module under direct sunlight or UV light and for best panel performance, unpack the cartons and start the production with the panels within one months after the reception of them.