Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 128064K - Y

Product Specification ***Version : 01***

28.08.2008

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2008/08/28	SPEC.

C O N T E N T S

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128X 64	dots
Module dimension (L*W*H)	70.9*41.86*2.01(MAX)	mm
View area	63.41*32.69	mm
Active area	61.41*30.69	mm
Dot size	0.45(W)X 0.45(H	mm
Dot pitch	0.48(W)X 0.48 (H	mm

(2) Controller IC: SSD1305 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Input Voltage (VDD)	VDD	-0.3	—	3.5	V
Supply Voltage (Vcc)	Vcc	8	—	16	V
Humidity	—	—	—	85	%
Operating lift time	—	—	30000(*)	—	Hrs

*:80cd/m^2 light on

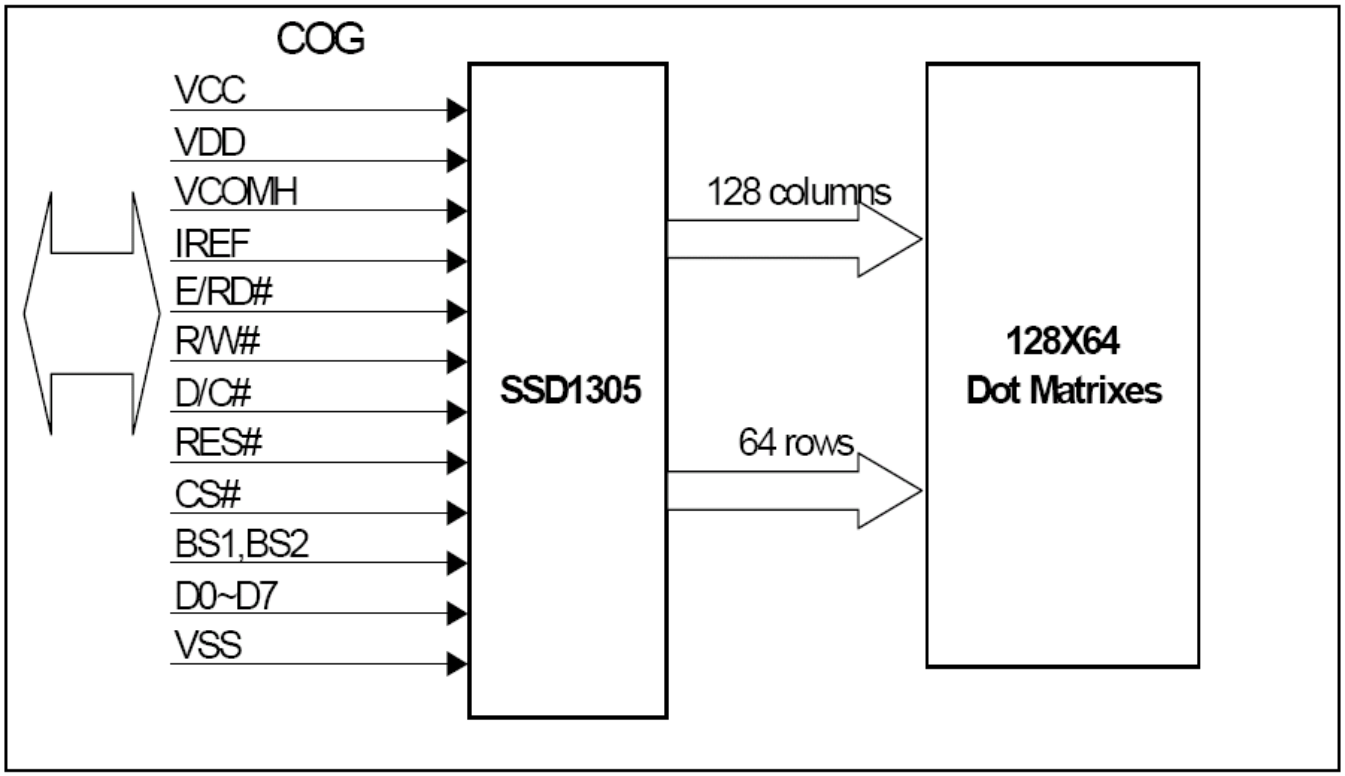
4. Electrical Characteristics

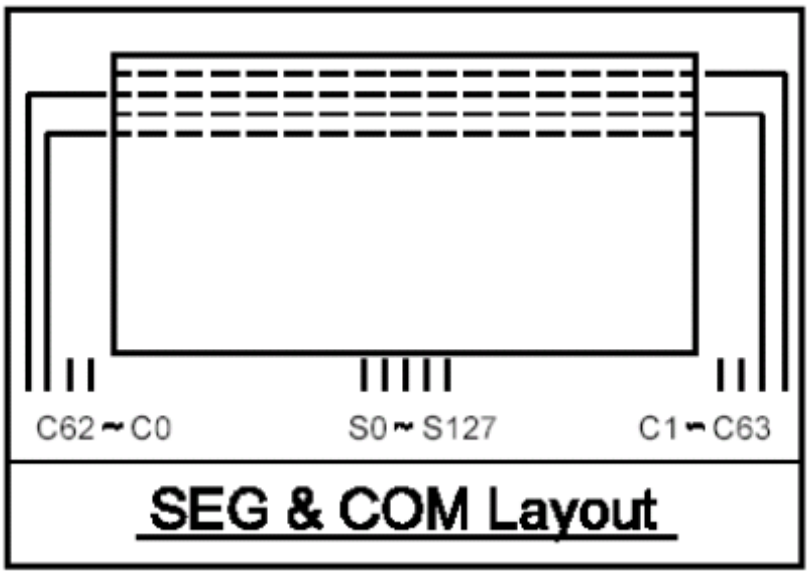
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	2.4	2.7	3.5	V
Supply Voltage For Panel	Vcc-Vss	—	14.5	15	15.5	V
Input High Vol	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	0.2V_{DD}	V
Output High Vol	V_{OH}	—	0.9V_{DD}	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	0	—	0.1V_{DD}	V
Supply Current	I_{DD}	—	—	28	30	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	us

6. Block Diagram





7. Interface Pin Function

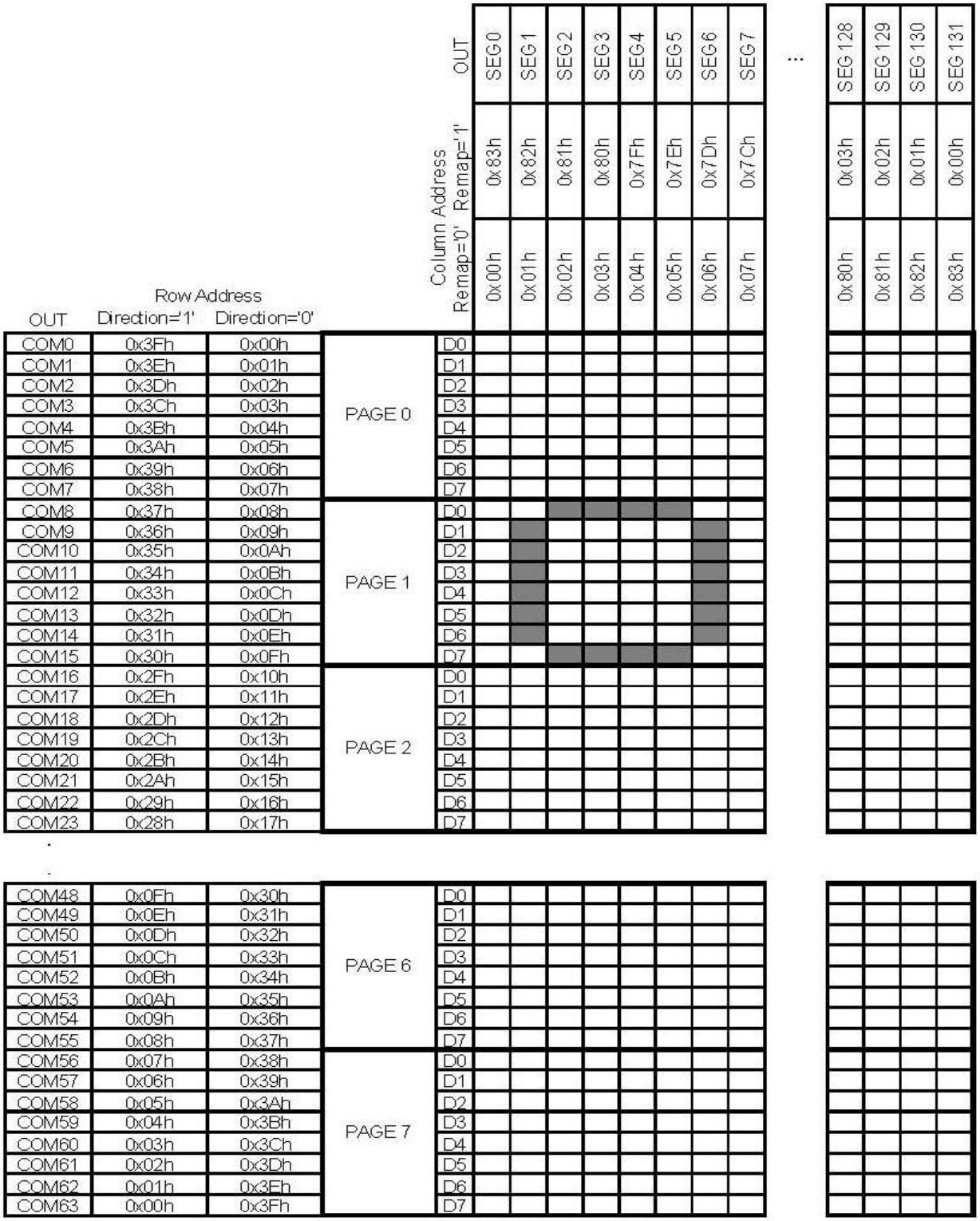
Pin No.	Symbol	Level	Description
1	Vcc	—	Positive OLED high voltage power supply
2	VCOMH	—	The COM voltage reference pin, this pin should be connected to ground through a capacitor
3	IREF	—	The current reference input pin, this pin should be connected to ground through a resistor.
4	DB7	H/L	Data bus line
5	DB6	H/L	Data bus line
6	DB5	H/L	Data bus line
7	DB4	H/L	Data bus line
8	DB3	H/L	Data bus line
9	DB2	H/L	Data bus line
10	DB1	H/L	Data bus line
11	DB0	H/L	Data bus line
12	E(RD)	H/L	Data read operation is initiated when it's pull low
13	R/W#	H/L	Data write operation is initiated when it's pull low
14	D/C#	H/L	This is data/command control pin, H: Data input ,L: Command input .
15	RES#	H/L	Hardware reset signal
16	CS#	H/L	Chip select pin. The driver IC will be selected When CS pin is active low.
17	BS2	H/L	Interface select pin
18	BS1	H/L	Interface select pin
19	VDD	H/L	Voltage power supply for logic
20	NC	—	No connection
21	Vss	—	This is ground pin
22	Vss	—	This is ground pin

8. Graphic Display Data RAM Address MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be display.

The size of the RAM is 132X64=8448bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.



9. Timing Characteristics

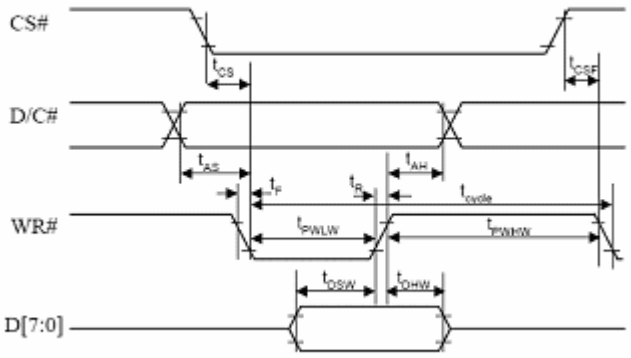
9-1.8080 MPU Interface

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = V_{DD}, T_A = 25°C)

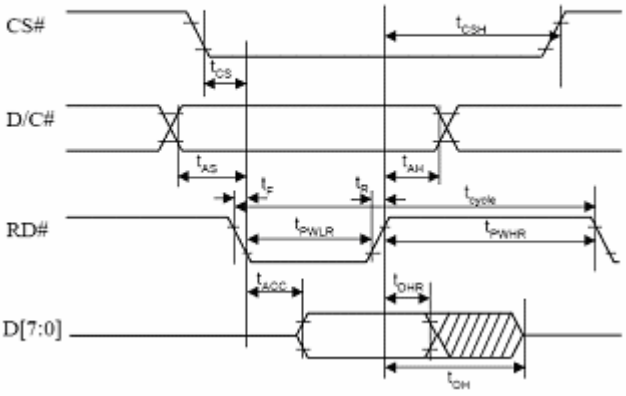
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)

Write cycle (Form 1)

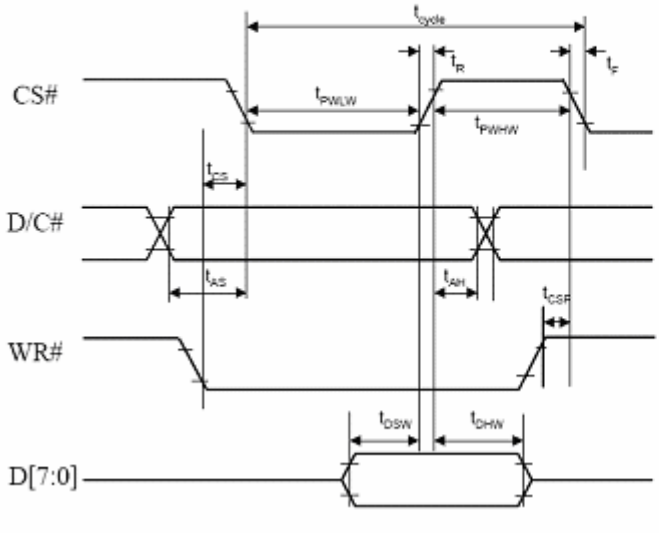


Read cycle (Form 1)

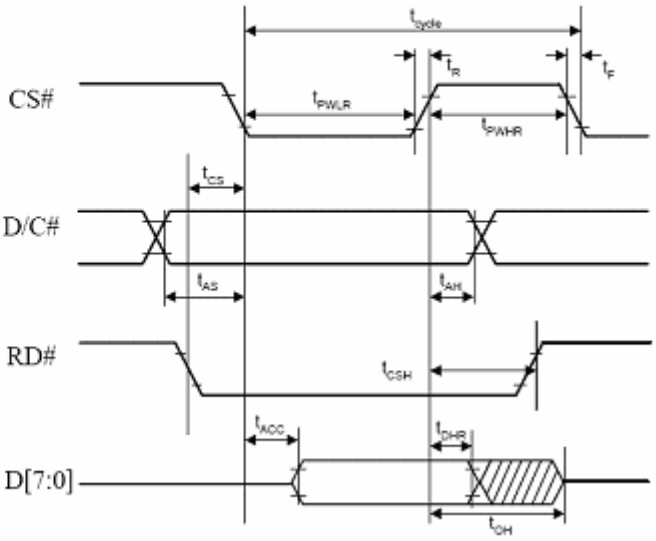


8080-series parallel interface characteristics (Form 2)

Write cycle (Form 2)



Read cycle (Form 2)

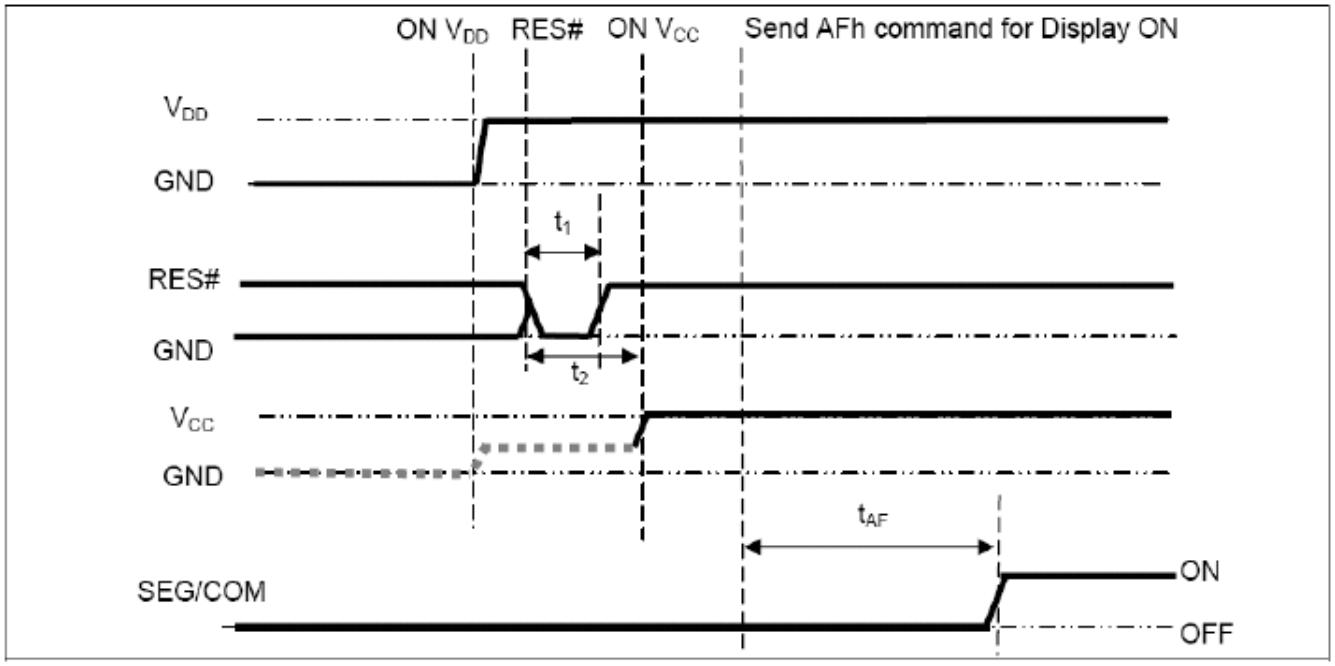


10. Power ON / OFF Sequence & Application Circuit

10.1 POWER ON / OFF SEQUENCE

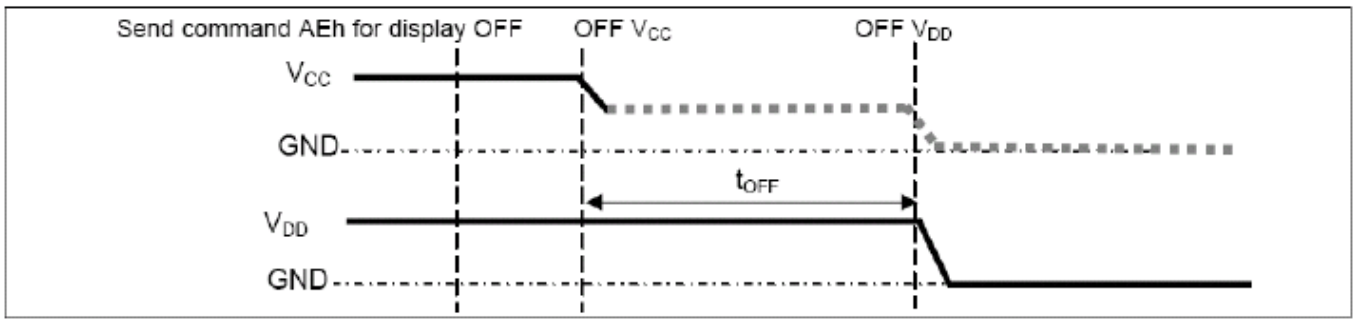
Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM wil be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

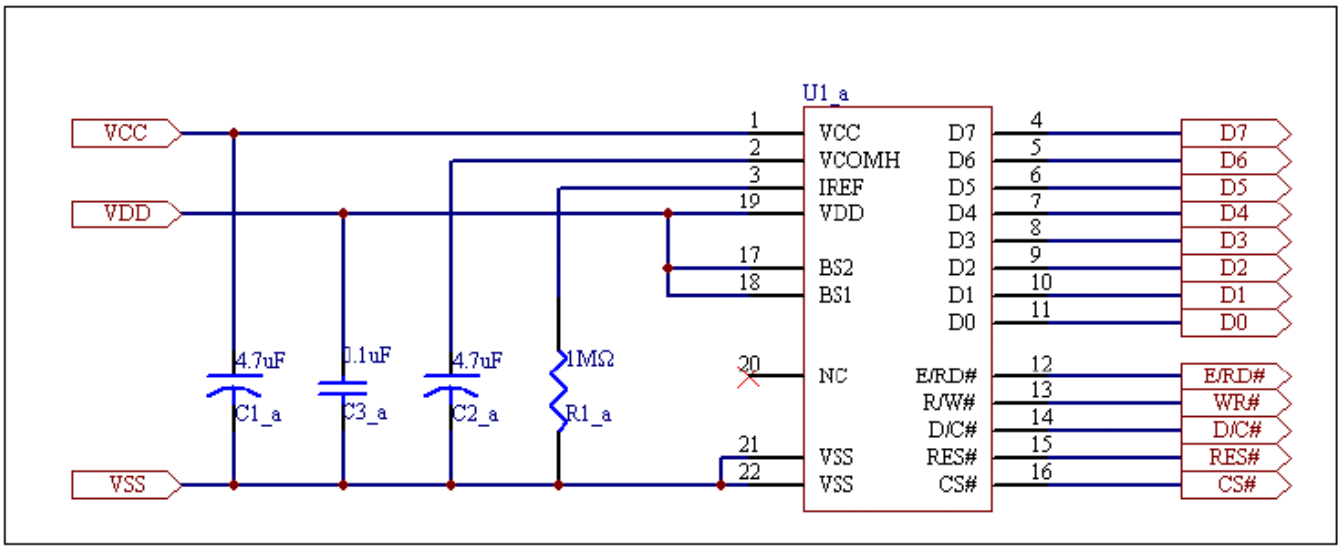


Note:

(1) Since an ESD protection circuit is connected between VDD and VCC,VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC in above figures.

(2)VCC should be disabled when it is OFF.

10.2 Application circuit



11. Display Control Instruction

Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-131d, (RESET=0d) B[7:0]: Column end address, range : 0-131d, (RESET =131d)
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control For BANK0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0 0	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Brightness For Area Color Banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0 0 0 0 0	91 X[5:0] A[5:0] B[5:0] C[5:0]	1 * * * *	0 * * * *	0 X_5 A_5 B_5 C_5	1 X_4 A_4 B_4 C_4	0 X_3 A_3 B_3 C_3	0 X_2 A_2 B_2 C_2	0 X_1 A_1 B_1 C_1	1 X_0 A_0 B_0 C_0	Set Look Up Table (LUT)	Set current drive pulse width of BANK0, Color A, B and C. BANK0: X[5:0] = 31… 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b) Color A: A[5:0] same as above (RESET = 111111b) Color B: B[5:0] same as above (RESET = 111111b) Color C: C[5:0] same as above (RESET = 111111b) **Note** (1) Color D pulse width is fixed at 64 clocks pulse.

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0 0 0	92 A[7:0] B[7:0] C[7:0] D[7:0]	1 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	0 A_5 B_5 C_5 D_5	1 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	0 A_2 B_2 C_2 D_2	1 A_1 B_1 C_1 D_1	0 A_0 B_0 C_0 D_0	Set Bank Color of BANK1 to BANK16 (PAGE0)	Set the bank color of BANK1~BANK16 to any one of the 4 colors : A, B, C and D . A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK1 A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK2 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK15 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK16
0 0 0 0 0	93 A[7:0] B[7:0] C[7:0] D[7:0]	1 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	0 A_5 B_5 C_5 D_5	1 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	0 A_2 B_2 C_2 D_2	1 A_1 B_1 C_1 D_1	1 A_0 B_0 C_0 D_0	Set Bank Color of BANK17~BANK32 (PAGE1)	Set the bank color of BANK17~BANK32 to any one of the 4 colors: A, B, C and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK17 A[3:2] : 00b, 01b, 10b, or 1b1 for Color = A, B, C or D of BANK18 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK31 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK32
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	X[0]=0b: column address 0 is mapped to SEG0 (RESET) X[0]=1b: column address 131 is mapped to SEG0
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	X_0=0b: Resume to RAM content display (RESET) Output follows RAM content X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel X[0]=1b: inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	AA	1	0	1	0	1	0	1	0	Reserved	Reserved
0 0 0 0	AB A[3:0] B[7:0] C[7:0]	1 * B_7 C_7	0 * B_6 C_6	1 * B_5 C_5	0 * B_4 C_4	1 A_3 B_3 C_3	0 A_2 B_2 C_2	1 A_1 B_1 C_1	1 A_0 B_0 C_0	Dim mode setting	A[3:0] : Reserved (set as 0000b) B [7:0] : Set contrast for BANK0, valid range 0-255d, please refer to command 81h C [7:0] : Set brightness for color bank, valid range 0-255d, please refer to command 82h

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 1	0 1	1 A_0	Master Configuration	A[0]=0b, Select external V_{CC} supply (RESET) A[0]=1b, Select internal DC-DC voltage converter **Note** (1) Refer to Section 8.11 for DC-DC converter details (2) The DC-DC converter must be enabled by the following command: ADh ; Master Configuration 8Fh ; Enable internal DC-DC AFh or ACh ; Display ON
0	AC AE AF	1	0	1	0	1	1	A_1	A_0	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) (RESET) AFh = Display ON in normal mode
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] X[3]=1b: remapped mode. Scan from COM[N~1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0~63. The value is reset to 00h after RESET.
0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b Range:0000b~1111b Frequency increases as setting value increases. Refer to section 10.1.23 for details.
0 0	D8	1 0	1 0	0 X_5	1 X_4	1 0	0 X_2	0 0	0 X_0	Set Area Color Mode ON/OFF & Low Power Display Mode	X[5:4]= 00b (RESET) : monochrome mode X[5:4]= 11b Area Color enable X[2]=0b and X[0]=0b: Normal power mode(RESET) X[2]=1b and X[0]=1b: Set low power display mode
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry A[7:4] : Phase 2 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	DA	1 0	1 0	0 X_5	1 X_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	X[4]=0b, Sequential COM pin configuration X[4]=1b(RESET), Alternative COM pin configuration X[5]=0b(RESET), Disable COM Left/Right remap X[5]=1b, Enable COM Left/Right remap Please refer to Table 10-3 for details.
0 0	DB A[5:2]	1 0	1 0	0 A_5	1 A_4	1 A_3	0 A_2	1 0	1 0	Set V_{COMH} Deselect Level	<table><tr><th>A[5:2]</th><th>Hex code</th><th>V_{COMH} deselect level</th></tr><tr><td>0000b</td><td>00h</td><td>~ 0.43 x V_{CC}</td></tr><tr><td>1101b</td><td>34h</td><td>~ 0.77 x V_{CC} (RESET)</td></tr><tr><td>1111b</td><td>3Ch</td><td>~ 0.83 x V_{CC}</td></tr></table>
0	E0	1	1	1	0	0	0	0	0	Enter Read Modify Write	Enter the Read Modify Write mode. Details please refer to section 10.1.28.
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0	EE	1	1	1	0	1	1	1	0	Exit Read Modify Write	Exit the Read Modify Write mode (Please refer to command E0h)

Graphic Acceleration Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Horizontal Scroll Setup	X[0]=0, Right Horizontal Scroll X[0]=1, Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 2 frame 011b – 128 frames | 111b – Invalid D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0]
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	X_1X_0=01b : Vertical and Right Horizontal Scroll X_1X_0=10b : Vertical and Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 2 frame 011b – 128 frames | 111b – Invalid D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		

Graphic Acceleration Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line (X5X4X3X2X1X0 of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls Please refer to Figure 10-14 for details.

Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserve D[6] : "1" for display OFF / "0" for display ON D[5] : Reserve D[4] : Reserve D[3] : Reserve D[2] : Reserve D[1] : Reserve D[0] : Reserve

Note

(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

12. Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and faces Cycles: 1	——
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	——

13. Appendix

13.1 Drawing