Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 256064B-W

Product Specification ***Version : 5***

05.02.2013

History of Version

Version	Contents	Date	Note
1	NEW VERSION	22.11.2008	SPEC.
2	Add contrast setting	09.11.2011	
3	UPDATE Quality Assurance、Reliability ADD Precautions for Handling、Precautions for Electrical、Precautions for Storage	17.08.2012	
4	Modify Cover page	17.10.2012	
5	Modify Quality Assurance	05.02.2013	

C O N T E N T S

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	256x64	dots
Module dimension (L*W*H)	87.4*64.5*2.01	mm
Active area	79.084*19.756	mm
Dot size	0.289(W)x0.289(H)	mm
Dot pitch	0.309(W)x0.309 (H)	mm
Color	White	

(2) Controller IC: SSD1322 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature	TOP		-40	—	+85	℃
Storage Temperature	TST		-40	—	+85	℃
Humidity					85	%
Supply Voltage For Logic	VDD		2.4	—	3.5	V
Supply Voltage For Panel	VCC		10		20	
Operating lift time		80cd/m², 50% checkerboard	13000(1)			Hrs
Operating lift time		70cd/m², 50% checkerboard	16000(2)			Hrs
Operating lift time		60cd/m², 50% checkerboard	19000(3)			Hrs

(A) Under VCC = 14V, Ta = 25℃, 50% RH.
(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.
(1) Setting of 80 cd/m²: Contrast setting : 0x70 Frame rate : 105Hz Duty setting : 1/64
(2) Setting of 70 cd/m²: Contrast setting : 0x5a Frame rate : 105Hz Duty setting : 1/64
(3) Setting of 60 cd/m²: Contrast setting : 0x49 Frame rate : 105Hz Duty setting : 1/64

4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	2.4	3.3	3.5	V
Supply Voltage For Panel	Vcc-V_{SS}	—	13.5	14	14.5	V
Input High Vol	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	0.2V_{DD}	V
Output High Vol	V_{OH}	—	0.9V_{DD}	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	0	—	0.1V_{DD}	V
Supply Current For Logic (with built-in positive voltage)	I_{DD}	—	—	270	—	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	us

6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	3.3V	Supply voltage for logic
3	CS	H/L	Chip select pin
4	/RES	H/L	Hardware Reset pin
5	D/C	H/L	H: Data; L: Command.
6	WR	H/L	write signal pin
7	RD	H/L	Read signal pin
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	DISF VCC	H/L H	DISF: VCC Voltage ON/OFF VCC: Supply Voltage For OLED

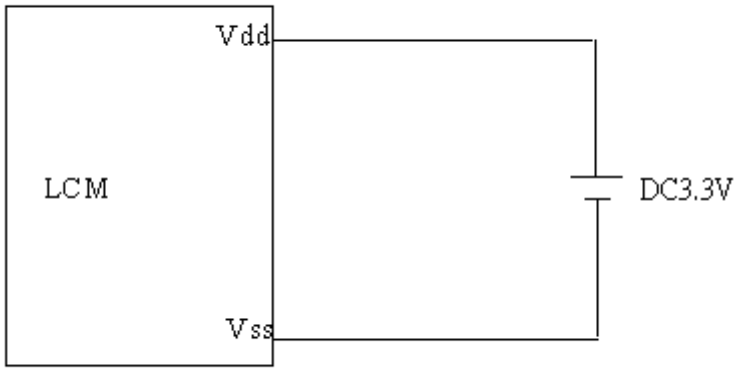
Default: Parallel 8-Bit 8080 Interface
68j : Parallel 8-Bit 6800 Interface Special Code
20i : SPI Interface Special Code

MCU interface assignment under different bus interface mode

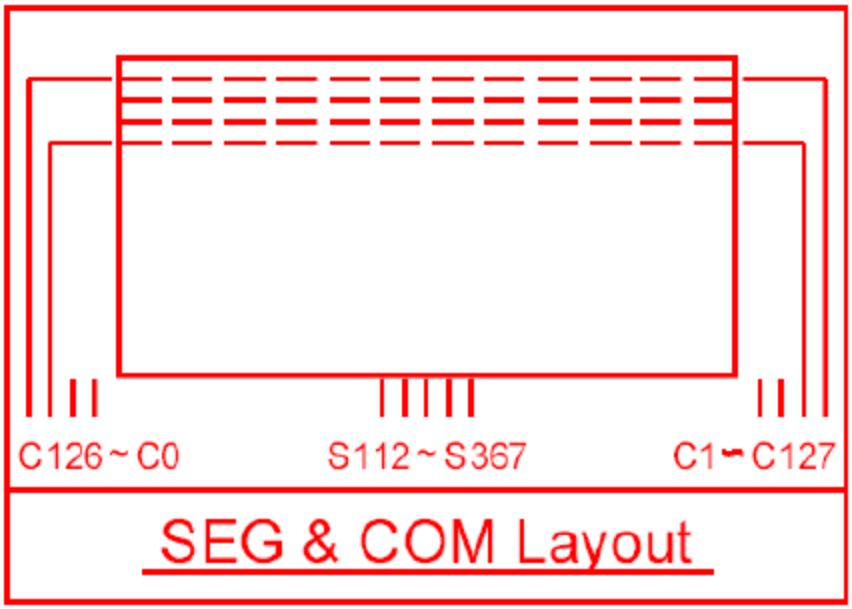
Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#

7. Power Supply For OLED Module And Panel Layout Diagram

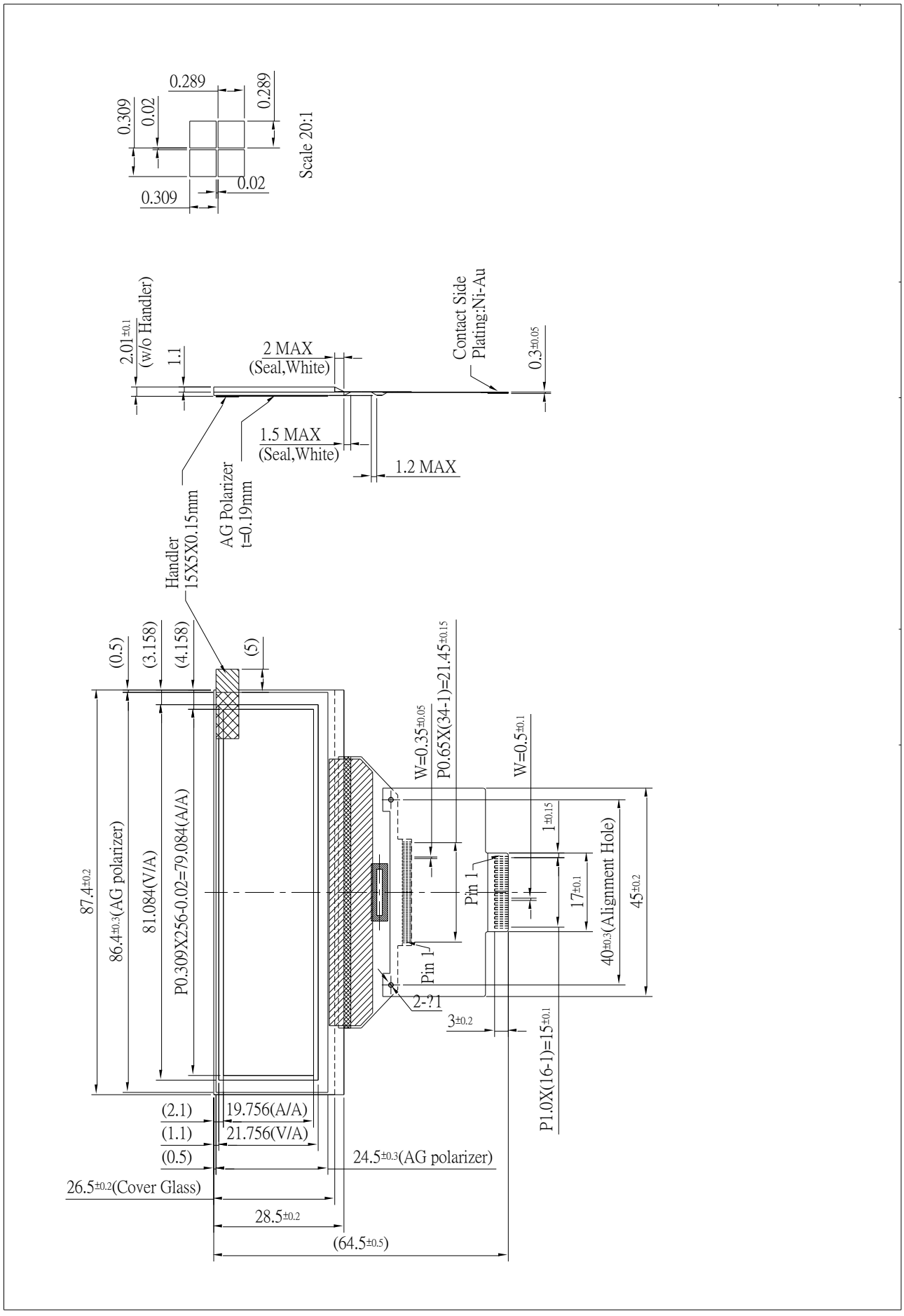
OLED Module operating on "DC 3.3V " input with built-in positive voltage



Panel Layout Diagram



8. Drawing


0.289
0.289
0.309
0.02
0.02
0.309
Scale 20:1
2.01±0.1
(w/o Handler)
1.1
2 MAX
(Seal,White)
Contact Side
Plating:Ni-Au
0.3±0.05
1.5 MAX
(Seal,White)
1.2 MAX
AG Polarizer
t=0.19mm
Handler
15X5X0.15mm
(0.5)
(3.158)
(4.158)
(5)
W=0.35±0.05
P0.65X(34-1)=21.45±0.15
W=0.5±0.1
1±0.15
Pin 1
17±0.1
40±0.3(Alignment Hole)
45±0.2
Pin 1
2-?1
3±0.2
P1.0X(16-1)=15±0.1
87.4±0.2
86.4±0.3(AG polarizer)
81.084(V/A)
P0.309X256-0.02=79.084(A/A)
(2.1)
19.756(A/A)
(1.1)
21.756(V/A)
(0.5)
24.5±0.3(AG polarizer)
26.5±0.2(Cover Glass)
28.5±0.2
(64.5±0.5)

9. SSD1322 controller data

9.1 Timing Characteristics

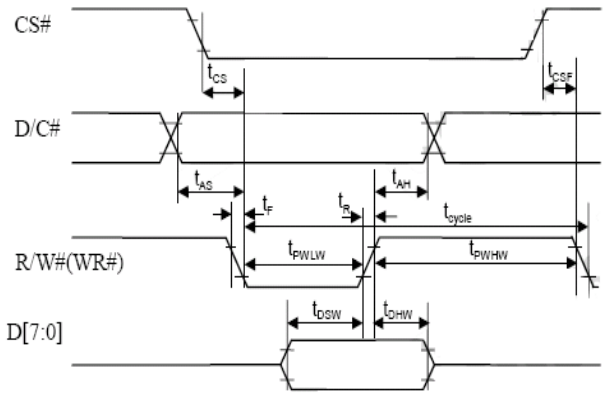
.8080 MPU Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

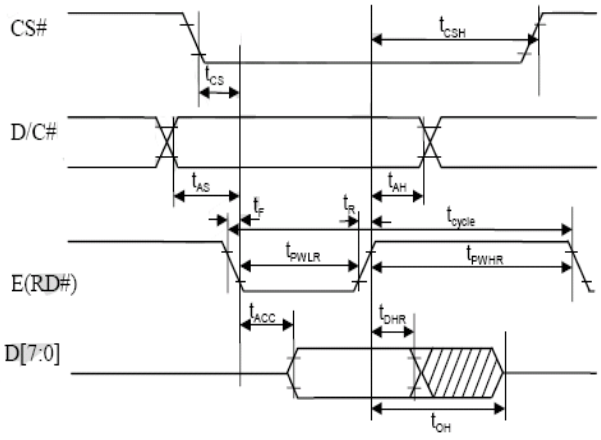
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle



Read cycle

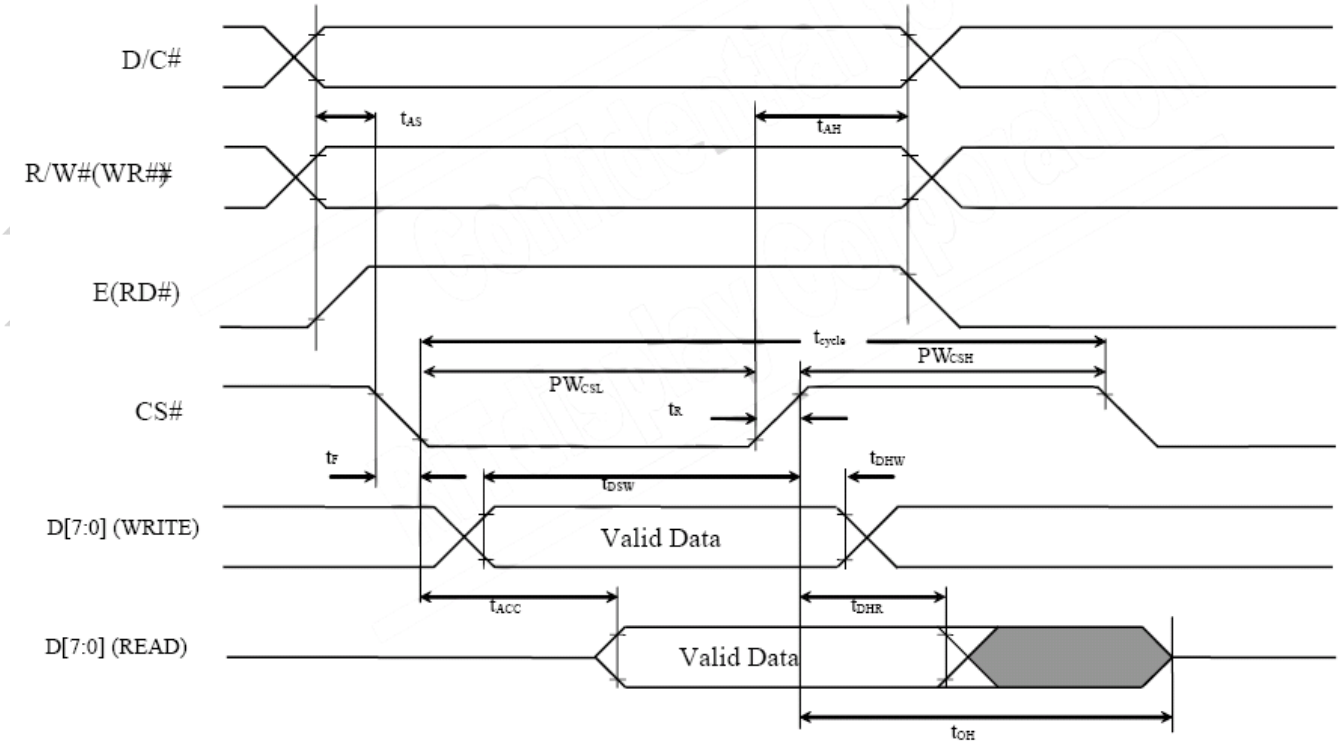


6800 MPU Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

6800-series MCU parallel interface characteristics

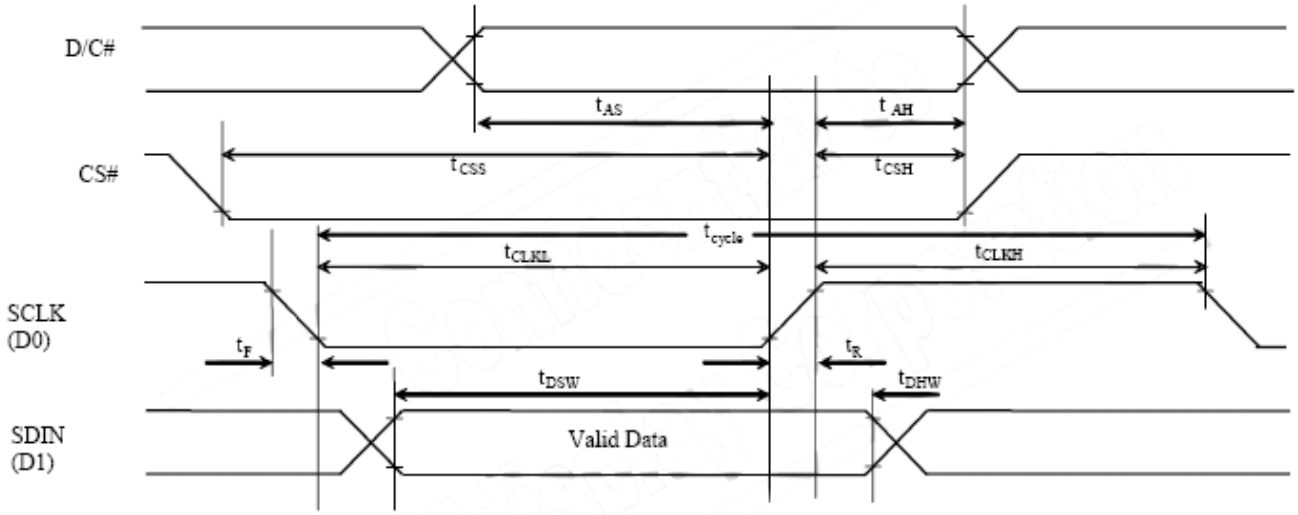


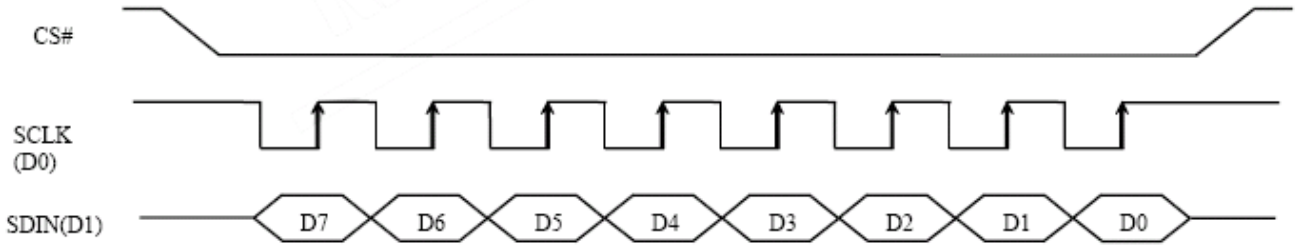
Serial Interface(4-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (4-wire SPI)



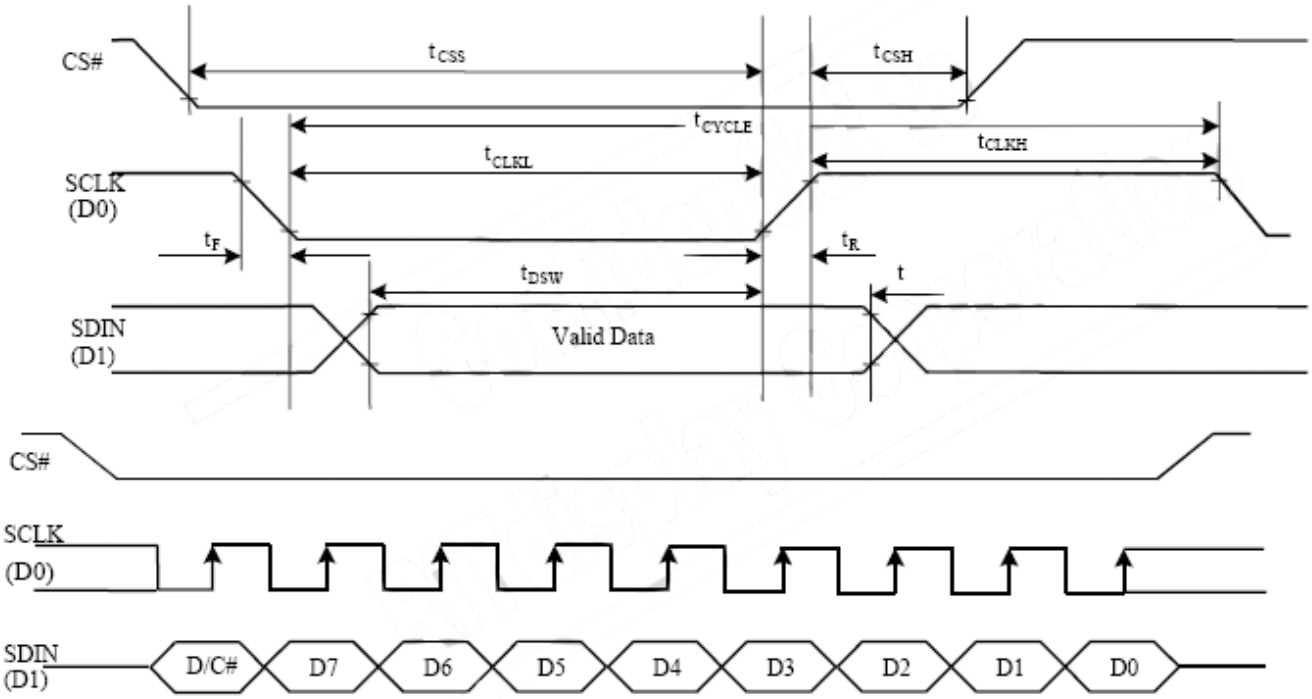


Serial Interface (3-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (3-wire SPI)



9.2 Display Control Instruction

(D/C#=0, R/W#(WR#) = 0, E(RD#)=1) unless specific setting is stated)

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A_5 0	0 A_4 B_4	0 0 0	0 A_2 0	0 A_1 0	0 A_0 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 00b, Disable Dual COM mode [reset] 01b, Enable Dual COM mode (MUX ≤ 63) **Note** (1) COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)
0 1 1	A8 A[6:0] B[6:0]	1 0 0	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	1 A_3 B_3	0 A_2 B_2	0 A_1 B_1	0 A_0 B_0	Enable Partial Display	This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must be ≥ A[6:0]
0	A9	1	0	1	0	1	0	0	1	Exit Partial Display	This command is sent to exit the Partial Display mode
0 1	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A_0	Function Selection	A[0]=0b, Select external V_{DD} A[0]=1b, Enable internal V_{DD} regulator [reset]
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow:

A[3:0]	Phase 1 period
0000	invalid
0001	invalid
0010	5 DCLKs
0011	7 DCLKs
0100	9 DCLKs [reset]
:	:
1111	31 DCLKs

A[7:4]	Phase 2 period
0000	invalid
0001	invalid
0010	invalid
0011	3 DCLKs
:	:
0111	7 DCLKs [reset]
:	:
1111	15 DCLKs

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>B3
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Front Clock Divider / Oscillator Frequency</td><td>A[3:0] [reset=0], divide by DIVSET where
<table><tr><th>A[3:0]</th><th>DIVSET</th></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>
A[7:4] Oscillator frequency, frequency increases as level increases [reset=1100b]</td></tr>
<tr><td>0
1
1</td><td>B4
A[1:0]
B[7:3]</td><td>1
1
B_7</td><td>0
0
B_6</td><td>1
1
B_5</td><td>1
0
B_4</td><td>0
0
B_3</td><td>1
0
1</td><td>0
A_1
0</td><td>0
A_0
1</td><td>Display Enhancement A</td><td>A[1:0] = 00b: Enable external VSL
A[1:0] = 10b: Internal VSL [reset]

B[7:3] = 11111b: Enhanced low GS display quality
B[7:3] = 10110b: Normal [reset]</td></tr>
<tr><td>0
1</td><td>B5
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set GPIO</td><td>A[1:0] GPIO0: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH

A[3:2] GPIO1: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH</td></tr>
<tr><td>0
1</td><td>B6
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Second Precharge Period</td><td>A[3:0] Second Pre-charge period
0000b 0 dclk
0001b 1 dclk
……
1000b 8 dclks [reset]
……
1111b 15 dclks</td></tr>
<tr><td>0
1
1
1
1
1
1
1</td><td>B8
A1[7:0]
A2[7:0]
.
.
.
A14[7:0]
A15[7:0]</td><td>1
$A1_7$
$A2_7$
.
.
.
$A14_7$
$A15_7$</td><td>0
$A1_6$
$A2_6$
.
.
.
$A14_6$
$A15_6$</td><td>1
$A1_5$
$A2_5$
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$A14_5$
$A15_5$</td><td>1
$A1_4$
$A2_4$
.
.
.
$A14_4$
$A15_4$</td><td>1
$A1_3$
$A2_3$
.
.
.
$A14_3$
$A15_3$</td><td>0
$A1_2$
$A2_2$
.
.
.
$A14_2$
$A15_2$</td><td>0
$A1_1$
$A2_1$
.
.
.
$A14_1$
$A15_1$</td><td>0
$A1_0$
$A2_0$
.
.
.
$A14_0$
$A15_0$</td><td>Set Gray Scale Table</td><td>The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d)

A1[7:0]: Gamma Setting for GS1,
A2[7:0]: Gamma Setting for GS2,
:
A14[7:0]: Gamma Setting for GS14,
A15[7:0]: Gamma Setting for GS15</td></tr>
</table>

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Note
[1] 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15

Refer to Section 8.8 for details

[2] The setting must be followed by the Enable Gray Scale Table command (00h)</td></tr>
<tr><td>0</td><td>B9</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Select Default Linear Gray Scale table</td><td>The default Linear Gray Scale table is set in unit of DCLK's as follow

GS0 level pulse width = 0;
GS1 level pulse width = 0;
GS2 level pulse width = 8;
GS3 level pulse width = 16;
:
:
GS14 level pulse width = 104;
GS15 level pulse width = 112

Refer to Section 8.8 for details</td></tr>
<tr><td>0
1</td><td>BB
A[4:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Pre-charge voltage</td><td>Set pre-charge voltage level [reset = 17h]
<table><tr><th>A[5:1]</th><th>Hex code</th><th>pre-charge voltage</th></tr><tr><td>00000</td><td>00h</td><td>0.20 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>11111</td><td>3Eh</td><td>0.60 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>BE
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>1
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set V_{COMH}</td><td>Set COM deselect voltage level [reset = 04h]
A[3:0] =
<table><tr><th>A[2:0]</th><th>Hex code</th><th>V_{COMH}</th></tr><tr><td>0000</td><td>00h</td><td>0.72 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>0100</td><td>04h</td><td>0.80 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>0111</td><td>07h</td><td>0.86 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>C1
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Contrast Current</td><td>A[7:0]: Contrast current value, range:00h~FFh,
i.e. 256 steps for I_{SEG} current [reset = 7Fh]</td></tr>
<tr><td>0
1</td><td>C7
A[3:0]</td><td>1
*</td><td>1
*</td><td>0
*</td><td>0
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Master Contrast Current Control</td><td>A[3:0] =
0000b, reduce output currents for all colors to 1/16
0001b, reduce output currents for all colors to 2/16
:
1110b, reduce output currents for all colors to 15/16
1111b, no change [reset]</td></tr>
<tr><td>0
1</td><td>CA
A[6:0]</td><td>1
*</td><td>1
A_6</td><td>0
A_5</td><td>0
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set MUX Ratio</td><td>A[6:0]: Set MUX ratio from 16MUX ~ 128MUX

A[6:0] = 15d represents 16MUX
:
A[6:0] = 127d represents 128MUX [reset]</td></tr>
</table>

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	D1	1	1	0	1	0	0	0	1		
1	A[5:4]	1	0	A_5	A_4	0	0	1	0	Display Enhancement B	A[5:4] = 00b: Reserved A[5:4] = 10b: Normal [reset]
1	20	0	0	1	0	0	0	0	0		
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command
1	A[2]	0	0	0	1	0	A_2	1	0		

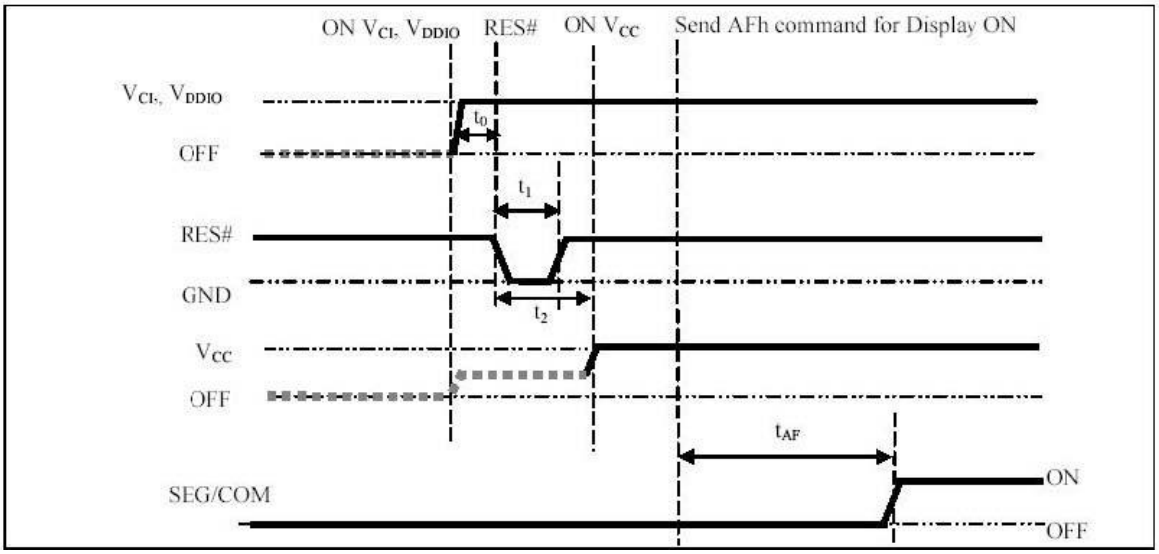
Note
(1) "*" stands for "Don't care".

9.3 Power ON / OFF Sequence & Application Circuit

POWER ON / OFF SEQUENCE

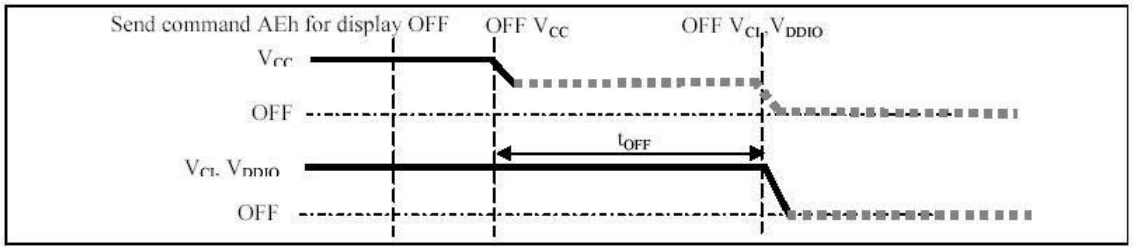
Power ON sequence:

1. Power ON VDD
2. After VDD become stable, set wait time at least 1ms (t0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 100us (t1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t2). Then Power ON VCC.(1)
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (tAF).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC.(1), (2)
3. Wait for tOFF. Power OFF VCI, VDDIO. (where Minimum tOFF=80ms (3), Typical tOFF=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC, VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC.
(2) VCC should be kept float (disable) when it is OFF.
(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.
(4) The register values are reset after t1.
(5) Power pins (VCI, VCC) can never be pulled to ground under any circumstance.

10 Quality Assurance

10.1 Inspection conditions

1. The inspection and meaurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5°C
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector≧30cm

10.2 Inspection Parameters

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm)
W</th><th>Length (mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜ W≦0.05</td><td>L≦3</td><td>3</td></tr>
<tr><td>0.05＜ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ≦0.2</td><td>Ignore</td></tr>
<tr><td>0.2＜Φ≦0.5</td><td>2</td></tr>
<tr><td>0.5＜Φ</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、
Lighting spot、
Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.15</td><td>2</td></tr>
<tr><td>0.15＜ D ≦0.2</td><td>1</td></tr>
<tr><td>0.2 ＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

10.3 WARRANTY POLICY

We will provide one-year warranty for the products only if under specification operating conditions.
If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.
We would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 13K hours.

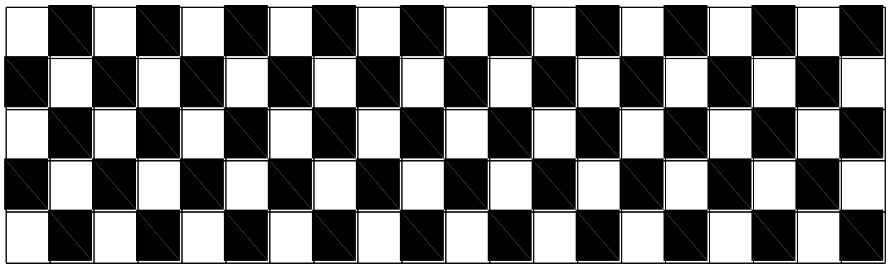
10.4.2 Test Condition:

10.4.2.1 Supply Voltage: Vcc=14V

10.4.2.2 Luminance: 80cd/m2

10.4.2.3 Operation temperature and humidity: 25 ℃ and 50%RH

10.4.2.4 Run-Patterns:



10.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.

11.Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption : within ±50% of initial value.

Reliability Test

Bolymin only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.

12.Precautions for Handling

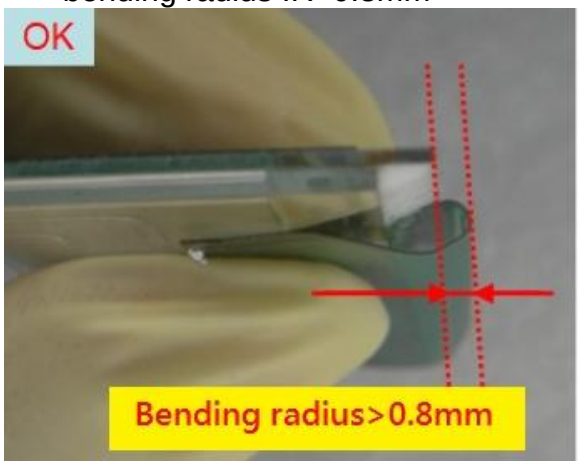
12.1 When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

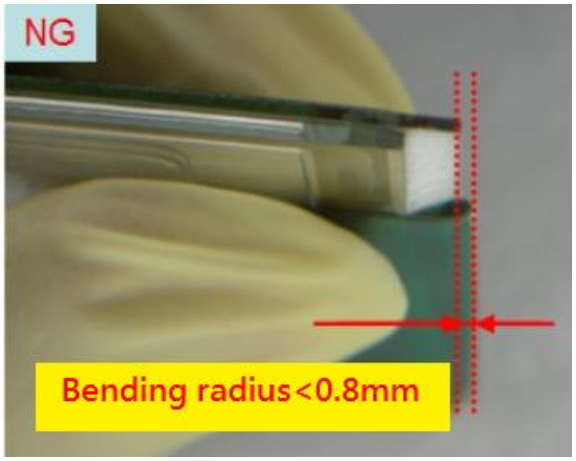
12.2 The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a height.

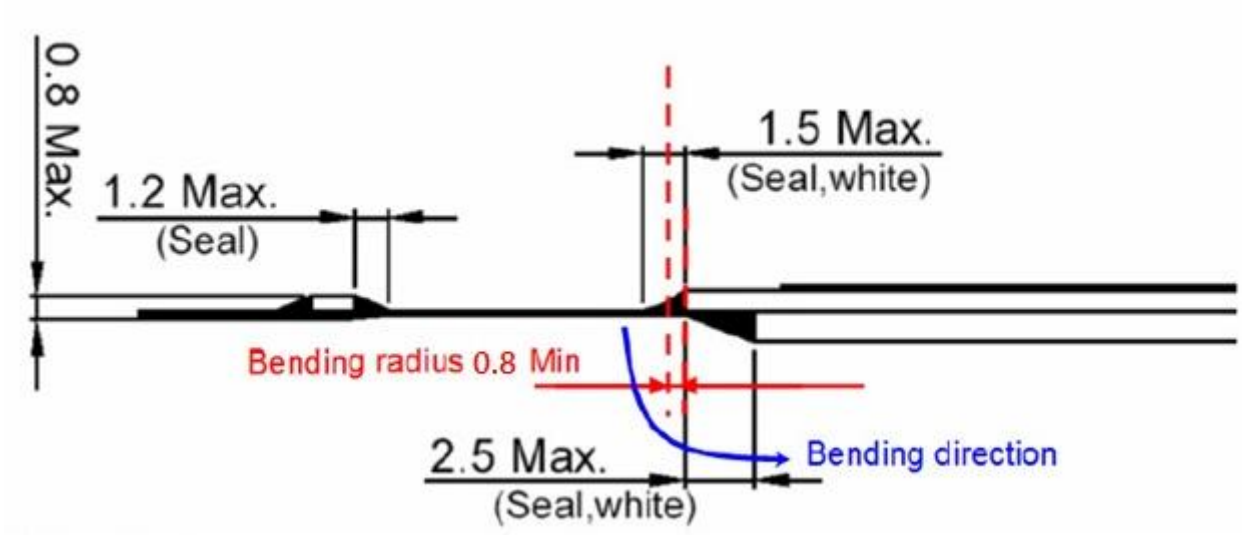
12.3 The OLED module is an electronic component and is subject to damage caused by Electro Static

Discharge (ESD) and hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. (See the photos below).

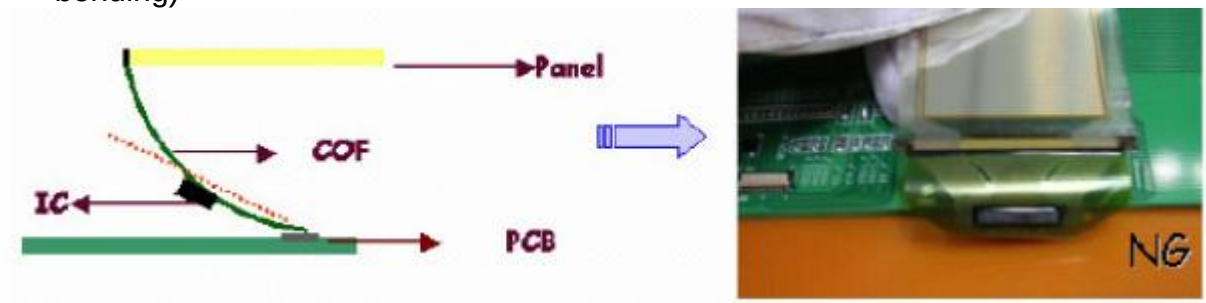
12.4 Please do not bend the film near the substrate glass.(this could cause film peeling and COF damage) and the peeling strength about 600g/cm, the bending <20times and the bending radius :R>0.8mm



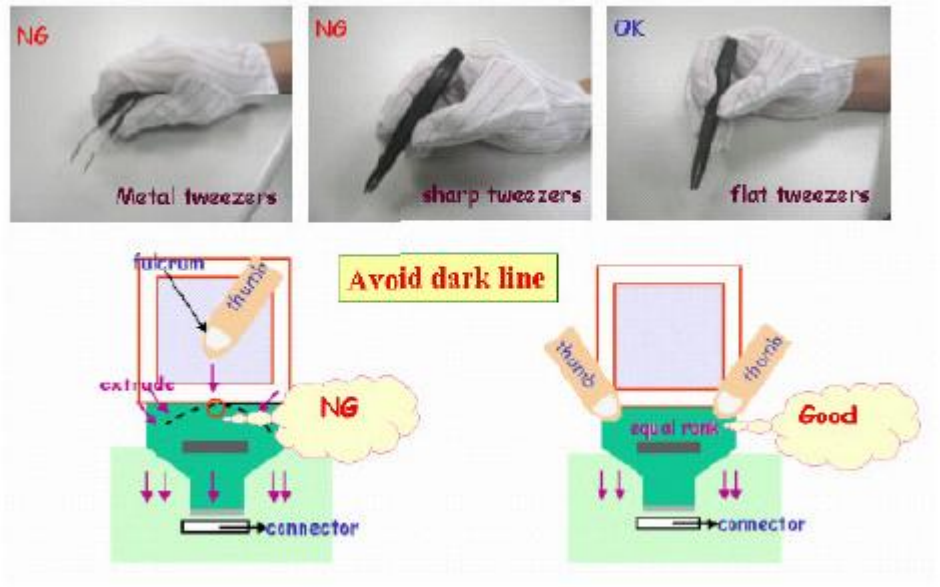




12.5 Avoid bending the film at IC bonding area.(>1.5mm)(this could damage the ILB bonding)



12.6 Use both thumbs to insert COF into the connector when assembling the panel. See the photo on the far right below for correct insertion of the film into the connector (one-handed insertion exerts uneven force on the film and could cause its breakage, photo on the left)



12.7 Do not wipe the pin of film with the dry or hard materials that will damage the surface. When cleaning the display surface, use soft cloth solvent and wipe gently (Recommend solvent: IPA, alcohol), and do not wipe the display with dry or hard materials that will damage the polarizer surface and do not use the solvent like: Water, Acetone, Aromatic

13. Precautions for Electrical

13.1. Design using the settings in the specification

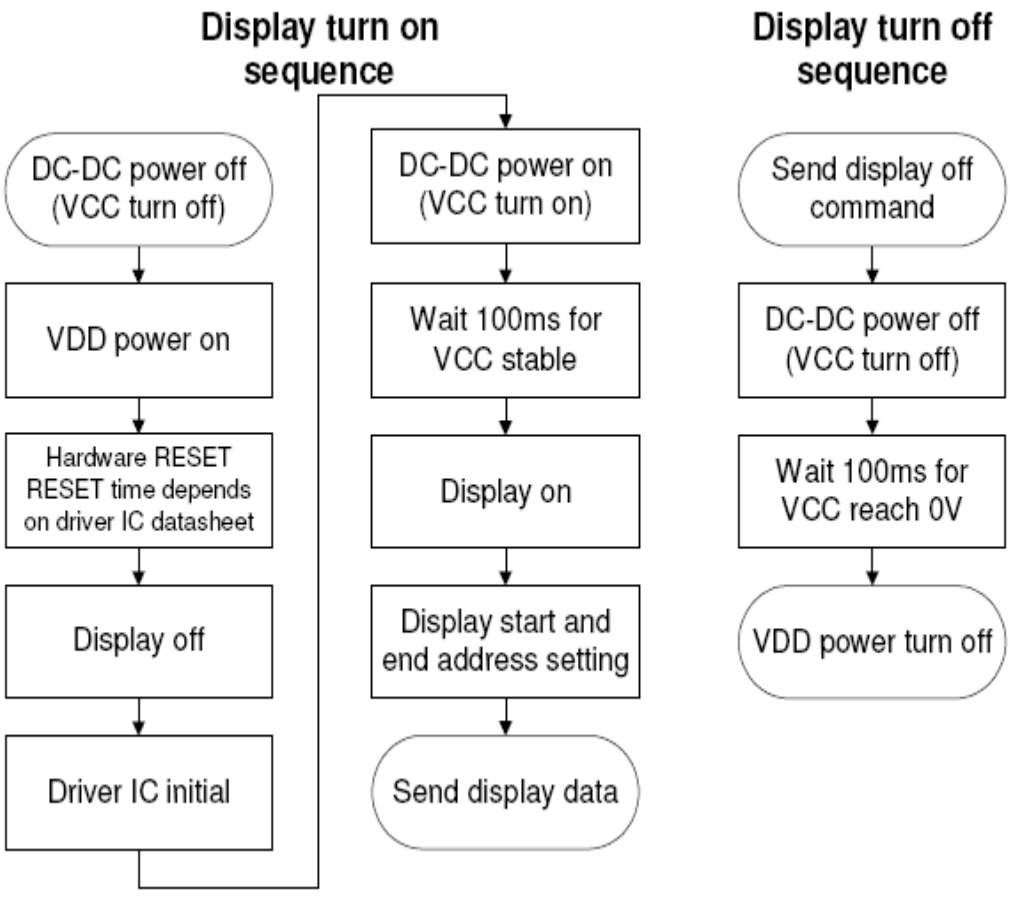
It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2. Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel malfunctioning.



13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode.

The power consumption is almost in direct proportion to the brightness of the panel, and also

in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

13.5.1 Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.

13.5.2 Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays

13.5.3 If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns

14. Precautions for Storage

Although the storage conditions and guarantee period are indicated in the specification, it is advisable to store the packed cartons or packages at 23℃±5℃,55%±10%RH, Do not store the OLED module under direct sunlight or UV light and for best panel performance, unpack the cartons and start the production with the panels within one months after the reception of them.