

HEF4081B

Quad 2-input AND gate

Rev. 04 — 26 May 2008

Product data sheet

1. General description

The HEF4081B is a quad 2-input AND gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity to output impedance variations.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input. The HEF4081B is suitable for use over both the industrial ($-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) and automotive ($-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$) temperature ranges.

2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Operates across the automotive temperature range from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

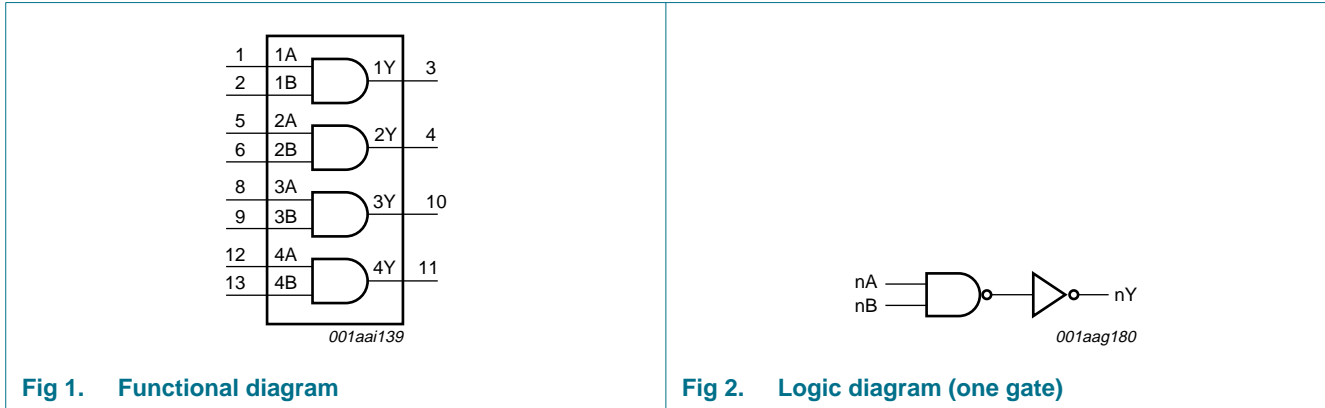
3. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

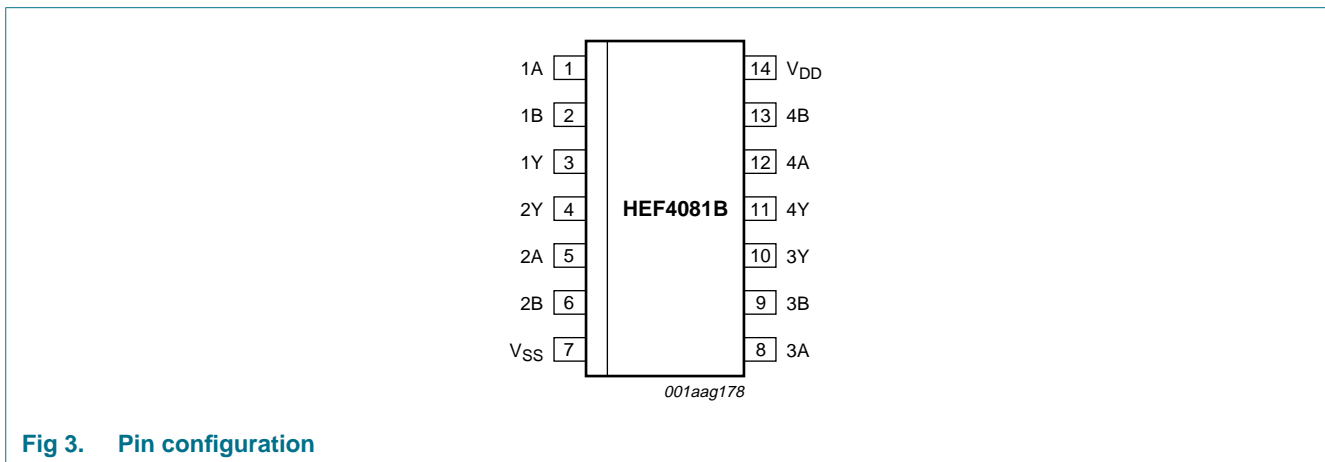
Type number	Package		
	Name	Description	Version
HEF4081BP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
HEF4081BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 5, 8, 12	input
1B to 4B	2, 6, 9, 13	input
1Y to 4Y	3, 4, 10, 11	output
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Output
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0\text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DD}	supply voltage		-0.5	+18	V	
I_{IK}	input clamping current	$V_I < 0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA	
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V	
I_{OK}	output clamping current	$V_O < 0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA	
$I_{I/O}$	input/output current		-	± 10	mA	
I_{DD}	supply current		-	50	mA	
T_{stg}	storage temperature		-65	+150	°C	
T_{amb}	ambient temperature		-40	+125	°C	
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to } +125\text{ °C}$				
		DIP14	[1]	-	750	mW
		SO14	[2]	-	500	mW
P	power dissipation	per output	-	100	mW	

[1] For DIP14 packages: above $T_{amb} = 70\text{ °C}$, P_{tot} derates linearly with 12 mW/K.

[2] For SO14 packages: above $T_{amb} = 70\text{ °C}$, P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	3.75	ns/V
		$V_{DD} = 10\text{ V}$	-	0.5	ns/V
		$V_{DD} = 15\text{ V}$	-	0.08	ns/V

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		$T_{amb} = +125\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-1.7	-	-1.4	-	-1.1	-	-1.1	-	mA
		$V_O = 4.6\text{ V}$	5 V	-0.64	-	-0.5	-	-0.36	-	-0.36	-	mA
		$V_O = 9.5\text{ V}$	10 V	-1.6	-	-1.3	-	-0.9	-	-0.9	-	mA
		$V_O = 13.5\text{ V}$	15 V	-4.2	-	-3.4	-	-2.4	-	-2.4	-	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.1	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{DD}	supply current	all valid input combinations; $I_O = 0\text{ A}$	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
C_I	input capacitance			-	-	-	7.5	-	-	-	pF	

10. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; $t_r = t_f \leq 20\text{ ns}$; waveforms see [Figure 4](#); test circuit see [Figure 5](#); unless otherwise specified. [1]

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	nA or nB to nY	5 V	$28 + 0.55 \times C_L$	-	55	110	ns
			10 V	$14 + 0.23 \times C_L$	-	25	50	ns
			15 V	$12 + 0.16 \times C_L$	-	20	40	ns
t _{PLH}	LOW to HIGH propagation delay	nA or nB to nY	5 V	$18 + 0.55 \times C_L$	-	45	90	ns
			10 V	$9 + 0.23 \times C_L$	-	20	40	ns
			15 V	$7 + 0.16 \times C_L$	-	15	30	ns
t _{THL}	HIGH to LOW output transition time		5 V	$10 + 1.0 \times C_L$	-	60	120	ns
			10 V	$9 + 0.42 \times C_L$	-	30	60	ns
			15 V	$6 + 0.28 \times C_L$	-	20	40	ns
t _{TLH}	LOW to HIGH output transition time		5 V	$10 + 1.00 \times C_L$	-	60	120	ns
			10 V	$9 + 0.42 \times C_L$	-	30	60	ns
			15 V	$6 + 0.28 \times C_L$	-	20	40	ns

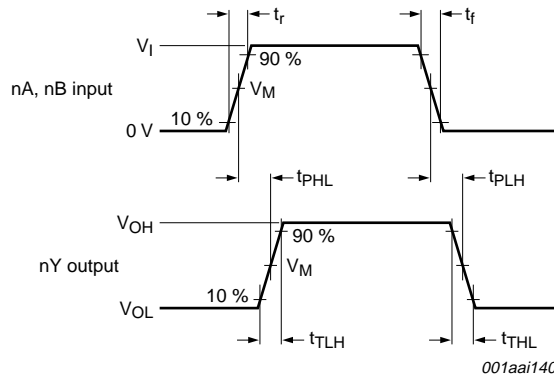
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 8. Dynamic power dissipation

$V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V _{DD}	Typical formula	where:
P _D	dynamic power dissipation	5 V	$P_D = 450 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	f_i = input frequency in MHz;
		10 V	$P_D = 2900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	f_o = output frequency in MHz;
		15 V	$P_D = 11700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.

11. Waveforms

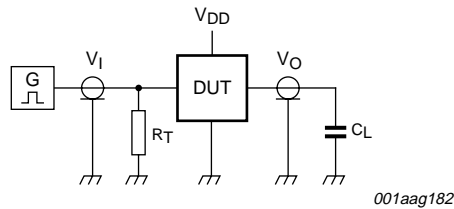


Measurement points are given in [Table 9](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).
 Definitions for test circuit:
 DUT = Device Under Test.
 C_L = load capacitance including jig and probe capacitance.
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 5. Test circuit

Table 10. Test data

Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	50 pF
		t_r, t_f
		≤ 20 ns

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

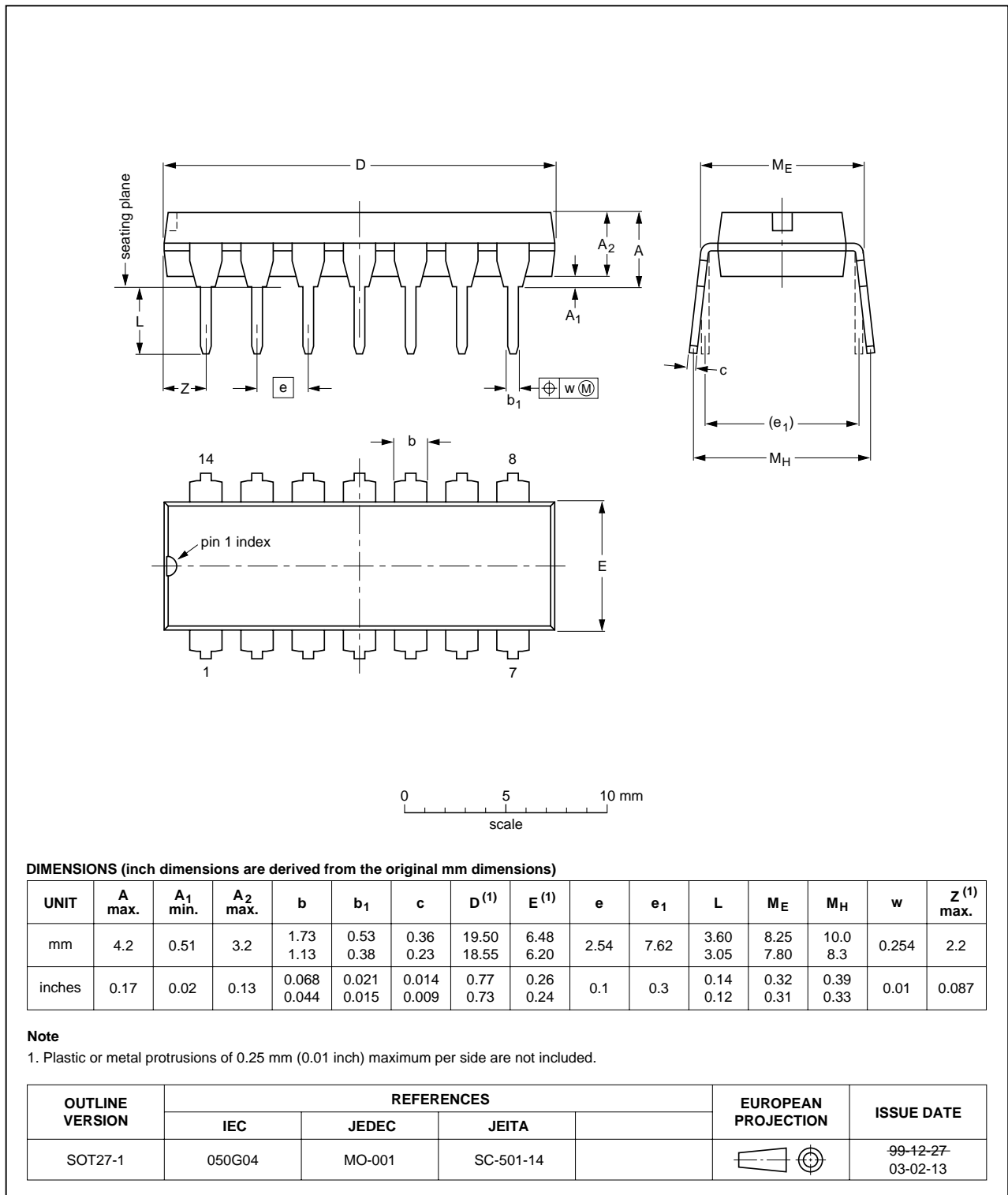


Fig 6. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

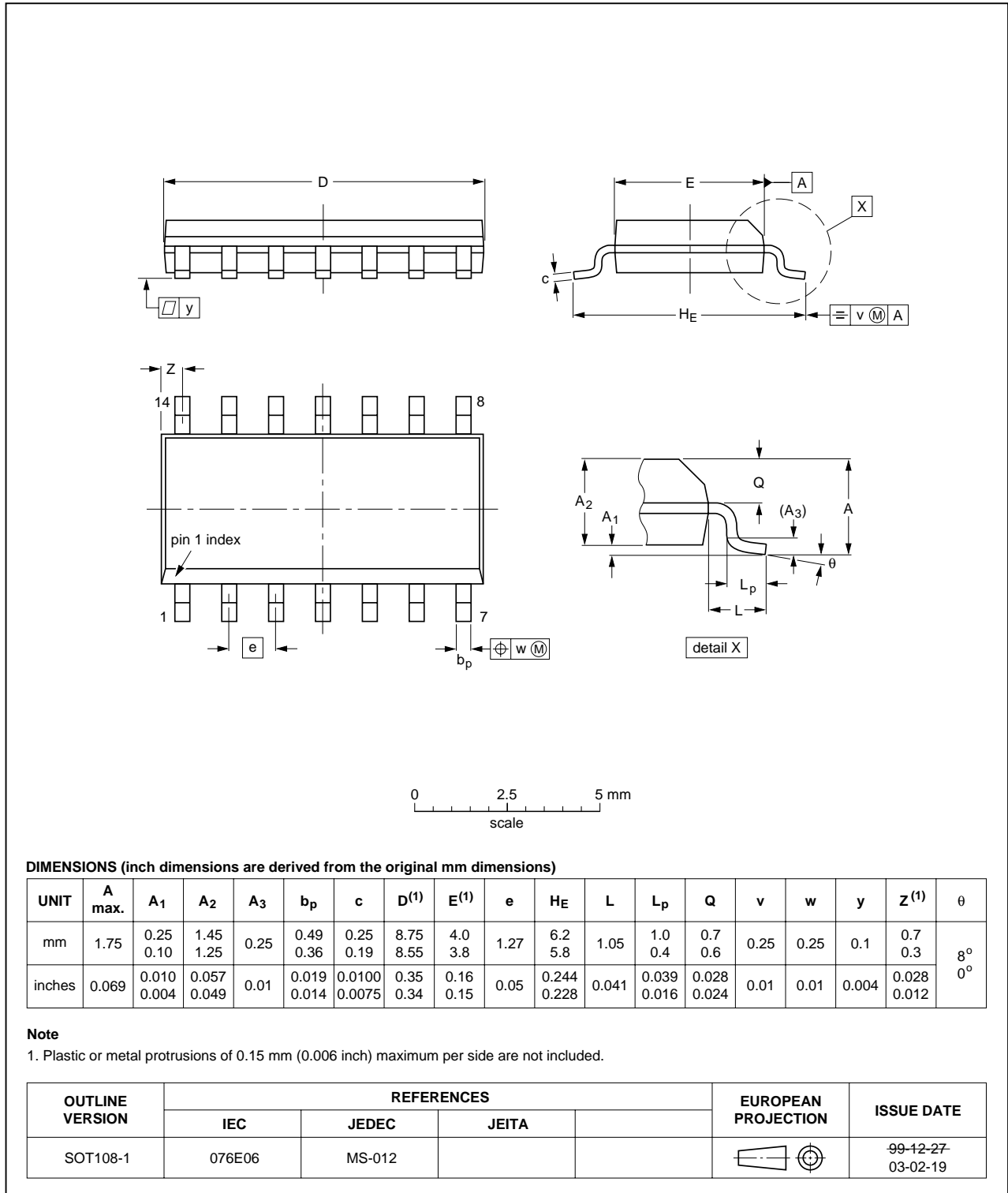


Fig 7. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4081B_4	20080526	Product data sheet	-	HEF4081B_CNV_3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Temperature range maximum increased from 85 °C to 125 °C throughout the data sheet. • Package SOT73 removed from Section 3 “Ordering information” and Section 12 “Package outline”. • Section 7 “Limiting values” and Table 6 “Static characteristics” added, taken from the HE4000B Family Specifications data sheet. • Section 9 “Static characteristics” I_{OH}, I_{OL}, I_I and I_{DD} values updated. • Typical temperature coefficient for propagation delays and output transitions removed. • Section 13 “Abbreviations” added. 			
HEF4081B_CNV_3	19950101	Product specification	-	HEF4081B_CNV_2
HEF4081B_CNV_2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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