



16-Channel Buffered CMOS Logic-Level Translators

General Description

The MAX13101E/MAX13102E/MAX13103E/MAX13108E 16-bit bidirectional CMOS logic-level translators provide the level shifting necessary to allow data transfer in multivoltage systems. These devices are inherently bidirectional due to their design and do not require the use of a direction input. Externally applied voltages, V_{CC} and V_L , set the logic levels on either side of the devices. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa.

The MAX13101E/MAX13102E/MAX13103E feature an enable input (EN) that, when low, reduces the V_{CC} and V_L supply currents to less than $2\mu A$. The MAX13108E features a multiplexing input (MULT) that selects one byte between the two, thus allowing multiplexing of the signals. The MAX13101E/MAX13102E/MAX13103E/MAX13108E have $\pm 15kV$ ESD protection on the I/O V_{CC} side for greater protection in applications that route signals externally. Three different output configurations are available during shutdown, allowing the I/O on the V_{CC} side or the V_L side to be put in a high-impedance state or pulled to ground through an internal $6k\Omega$ resistor.

The MAX13101E/MAX13102E/MAX13103E/MAX13108E accept V_{CC} voltages from +1.65V to +5.5V and V_L voltages from +1.2V to V_{CC} , making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX13101E/MAX13102E/MAX13103E/MAX13108E are available in 36-bump UCSP™ and 40-pin TQFN packages, and operate over the extended $-40^\circ C$ to $+85^\circ C$ temperature range.

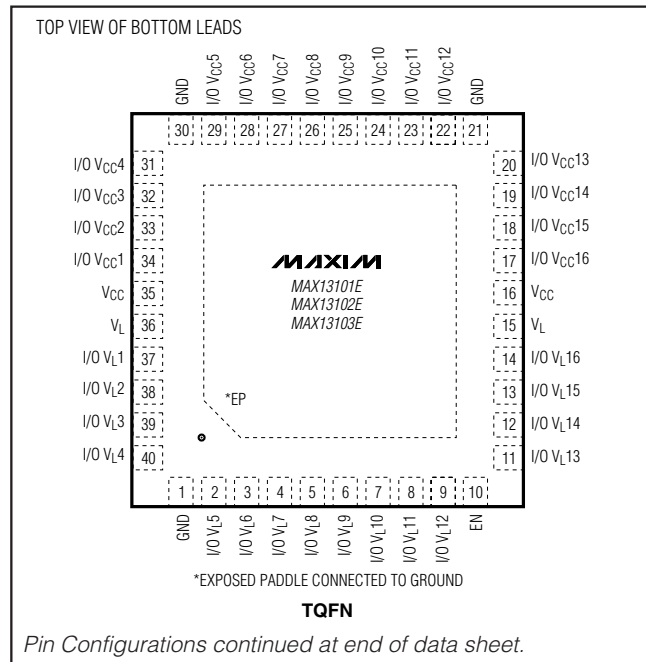
Applications

CMOS Logic-Level Translation	PDA's
Portable Equipment	Digital Still Cameras
Cell Phones	Smart Phones

Features

- ◆ Wide Supply Voltage Range
 V_{CC} Range of 1.65V to 5.5V
 V_L Range of 1.2V to V_{CC}
- ◆ ESD Protection on I/O V_{CC} Lines
 $\pm 15kV$ Human Body Model
- ◆ Up to 20Mbps Throughput
- ◆ Low $0.03\mu A$ Typical Quiescent Current
- ◆ UCSP and TQFN Packages

Pin Configurations



Ordering Information/Selector Guide

PART	PIN-PACKAGE	DATA RATE (Mbps)	I/O V_L STATE DURING SHUTDOWN	I/O V_{CC} STATE DURING SHUTDOWN	MULTIPLEXER FEATURE	PKG CODE
MAX13101EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	$6k\Omega$ to GND	No	B36-1
MAX13101EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	$6k\Omega$ to GND	No	T4055-1

Note: All devices operate over the $-40^\circ C$ to $+85^\circ C$ operating temperature range.

*Future product—contact factory for availability.

**UCSP bumps are in a 6 x 6 array.

Ordering Information/Selector Guide continued at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

16-Channel Buffered CMOS Logic-Level Translators

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V _{CC}	-0.3V to +6V
V _L	-0.3V to +6V
I/O V _{CC}	-0.3V to (V _{CC} + 0.3V)
I/O V _L	-0.3V to (V _L + 0.3V)
EN, MULT	-0.3V to +6V
Short-Circuit Duration I/O V _L , I/O V _{CC} to GND	Continuous
Continuous Power Dissipation (T _A = +70°C)	
36-Bump UCSP (derate 17.0mW/°C above +70°C) ..	1361mW
40-Pin TQFN (derate 35.7mW/°C above +70°C)	2857mW

Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX13101E/MAX13102E/MAX13103E), MULT = V_L or GND (MAX13108E), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V _L Supply Range	V _L		1.2		V _{CC}	V
V _{CC} Supply Range	V _{CC}		1.65		5.50	V
Supply Current from V _{CC}	I _{QVCC}	I/O V _{CC} = GND, I/O V _L = GND or I/O V _{CC} = V _{CC} , I/O V _L = V _L , EN = V _L , MULT = GND or V _L		0.03	10	μA
Supply Current from V _L	I _{QVL}	I/O V _{CC} = GND, I/O V _L = GND or I/O V _{CC} = V _{CC} , I/O V _L = V _L , EN = V _L , MULT = GND or V _L		0.03	20	μA
V _{CC} Shutdown Supply Current	I _{SHDN-VCC}	T _A = +25°C, EN = GND, I/O V _{CC} = GND, I/O V _L = GND, MAX13101E/MAX13102E/MAX13103E		0.03	1	μA
V _L Shutdown Supply Current	I _{SHDN-VL}	T _A = +25°C, EN = GND, I/O V _{CC} = GND, I/O V _L = GND, MAX13101E/MAX13102E/MAX13103E		0.03	2	μA
I/O V _{CC} Tri-State Output Leakage Current		T _A = +25°C, EN = GND, MAX13102E/MAX13103E		0.02	1	μA
		T _A = +25°C, MULT = GND (I/O V _{CC} 1 - I/O V _{CC} 8) or MULT = V _L (I/O V _{CC} 9 - I/O V _{CC} 16) MAX13108E		0.02	1	
I/O V _L Tri-State Output Leakage Current		T _A = +25°C, EN = GND, MAX13101E/ MAX13103E		0.02	1	μA
		T _A = +25°C, MULT = GND (I/O V _L 1 - I/O V _L 8) or MULT = V _L (I/O V _L 9 - I/O V _L 16) MAX13108E		0.02	1	
I/O V _L Pull-down Resistance During Shutdown		EN = GND, MAX13102E	4		10	kΩ

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +1.65V$ to $+5.5V$, $V_L = +1.2V$ to V_{CC} , $EN = V_L$ (MAX13101E/MAX13102E/MAX13103E), $MULT = V_L$ or GND (MAX13108E), $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +1.65V$, $V_L = +1.2V$, $T_A = +25^\circ C$.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC_}$ Pulldown Resistance During Shutdown		$EN = GND$, MAX13101E	4		10	$k\Omega$
EN or MULT Input Leakage Current		$T_A = +25^\circ C$			1	μA
LOGIC-LEVEL THRESHOLDS						
I/O $V_L_$ Input-Voltage High Threshold	V_{IHL}				$2/3 \times V_L$	V
I/O $V_L_$ Input-Voltage Low Threshold	V_{ILL}		$1/3 \times V_L$			V
I/O $V_{CC_}$ Input-Voltage High Threshold	V_{IHC}				$2/3 \times V_{CC}$	V
I/O $V_{CC_}$ Input-Voltage Low Threshold	V_{ILC}		$1/3 \times V_{CC}$			V
EN, MULT Input-Voltage High Threshold	$V_{IH-SHDN}$				$V_L - 0.4$	V
EN, MULT Input-Voltage Low Threshold	$V_{IL-SHDN}$		0.4			V
I/O $V_L_$ Output-Voltage High	V_{OHL}	I/O $V_L_$ source current = $20\mu A$, I/O $V_{CC_} \geq V_{IHC}$	$V_L - 0.4$			V
I/O $V_L_$ Output-Voltage Low	V_{OLL}	I/O $V_L_$ sink current = $20\mu A$, I/O $V_{CC_} \leq V_{ILC}$			0.4	V
I/O $V_{CC_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC_}$ source current = $20\mu A$, I/O $V_L_ \geq V_{IHL}$	$V_{CC} - 0.4$			V
I/O $V_{CC_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC_}$ sink current = $20\mu A$, I/O $V_L_ \leq V_{ILL}$			0.4	V
RISE/FALL-TIME ACCELERATOR STAGE						
Transition-Detect Threshold		I/O V_{CC} side			$V_{CC} / 2$	V
		I/O V_L side			$V_L / 2$	
Accelerator Pulse Duration		$V_L = 1.2V$, $V_{CC} = 1.65V$		20		ns
I/O $V_L_$ Output-Accelerator Sink Impedance		$V_L = 1.2V$, $V_{CC} = 1.65V$		60		Ω
		$V_L = 5V$, $V_{CC} = 5V$		5		
I/O $V_{CC_}$ Output-Accelerator Sink Impedance		$V_L = 1.2V$, $V_{CC} = 1.65V$		15		Ω
		$V_L = 5V$, $V_{CC} = 5V$		5		
I/O $V_L_$ Output-Accelerator Source Impedance		$V_L = 1.2V$, $V_{CC} = 1.65V$		30		Ω
		$V_L = 5V$, $V_{CC} = 5V$		5		
I/O $V_{CC_}$ Output-Accelerator Source Impedance		$V_L = 1.2V$, $V_{CC} = 1.65V$		20		Ω
		$V_L = 5V$, $V_{CC} = 5V$		7		
ESD PROTECTION						
I/O $V_{CC_}$		Human Body Model		± 15		kV

MAX13101E/MAX13102E/MAX13103E/MAX13108E

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TIMING CHARACTERISTICS

($V_{CC} = +1.65V$ to $+5.5V$, $V_L = +1.2V$ to V_{CC} , $EN = V_L$ (MAX13101E/MAX13102E/MAX13103E), $MULT = V_L$ or GND (MAX13108E), $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +1.65V$, $V_L = +1.2V$, $T_A = +25^\circ C$.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V_L _ Rise Time	t_{RVL}	$R_S = 50\Omega$, $C_{I/OVL_} = 15pF$, $t_{RISE} \leq 3ns$, (Figures 2a, 2b)			15	ns
I/O V_L _ Fall Time	t_{FVL}	$R_S = 50\Omega$, $C_{I/OVL_} = 15pF$, $t_{FALL} \leq 3ns$, (Figures 2a, 2b)			15	ns
I/O V_{CC} _ Rise Time	t_{RVCC}	$R_S = 50\Omega$, $C_{I/OVCC_} = 50pF$, $t_{RISE} \leq 3ns$, (Figures 1a, 1b)			15	ns
I/O V_{CC} _ Fall Time	t_{FVCC}	$R_S = 50\Omega$, $C_{I/OVCC_} = 50pF$, $t_{FALL} \leq 3ns$, (Figures 1a, 1b)			15	ns
Propagation Delay (Driving I/O V_L _)	$t_{PVL-VCC}$	$R_S = 50\Omega$, $C_{I/OVCC_} = 50pF$, $t_{RISE} \leq 3ns$, (Figures 1a, 1b)			20	ns
Propagation Delay (Driving I/O V_{CC} _)	$t_{PVCC-VL}$	$R_S = 50\Omega$, $C_{I/OVL_} = 15pF$, $t_{RISE} \leq 3ns$, (Figures 2a, 2b)			20	ns
Channel-to-Channel Skew	t_{SKEW}	$R_S = 50\Omega$, $C_{I/OVCC_} = 50pF$, $C_{I/OVL_} = 15pF$, $t_{RISE} \leq 3ns$			5	ns
Part-to-Part Skew	t_{PPSKEW}	$R_S = 50\Omega$, $C_{I/OVCC_} = 50pF$, $C_{I/OVL_} = 15pF$, $t_{RISE} \leq 3ns$, $\Delta T_A = +20^\circ C$ (Notes 3, 4)			10	ns
Propagation Delay from I/O V_L _ to I/O V_{CC} _ After EN	t_{EN-VCC}	$C_{I/OVCC_} = 50pF$ (Figure 3)			1	μs
Propagation Delay from I/O V_{CC} _ to I/O V_L _ After EN	t_{EN-VL}	$C_{I/OVL_} = 15pF$ (Figure 4)			1	μs
Maximum Data Rate		$R_{SOURCE} = 50\Omega$, $C_{I/OVCC_} = 50pF$, $C_{I/OVL_} = 15pF$, $t_{RISE} \leq 3ns$	20			Mbps

Note 1: All units are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 2: For normal operation, ensure that $V_L < (V_{CC} + 0.3V)$. During power-up, $V_L > (V_{CC} + 0.3V)$ does not damage the device.

Note 3: V_{CC} from device 1 must equal V_{CC} of device 2. V_L from device 1 must equal V_L of device 2.

Note 4: Guaranteed by design, not production tested.

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Test Circuits/Timing Diagrams

MAX13101E/MAX13102E/MAX13103E/MAX13108E

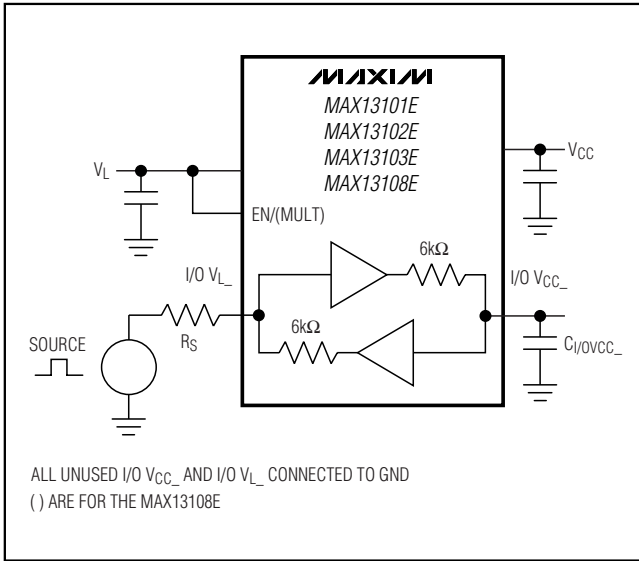


Figure 1a. Driving I/O VL_

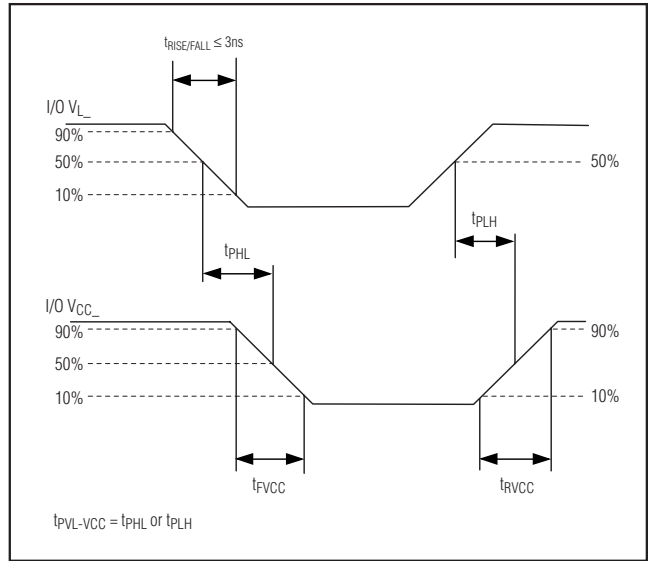


Figure 1b. Timing for Driving I/O VL_

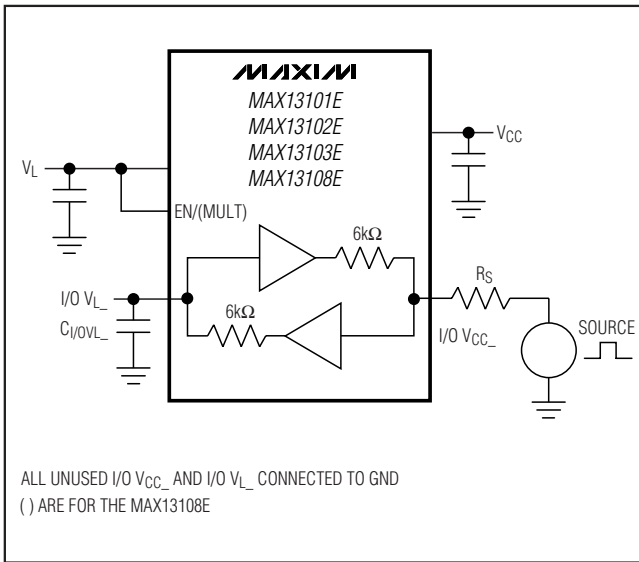


Figure 2a. Driving I/O VCC_

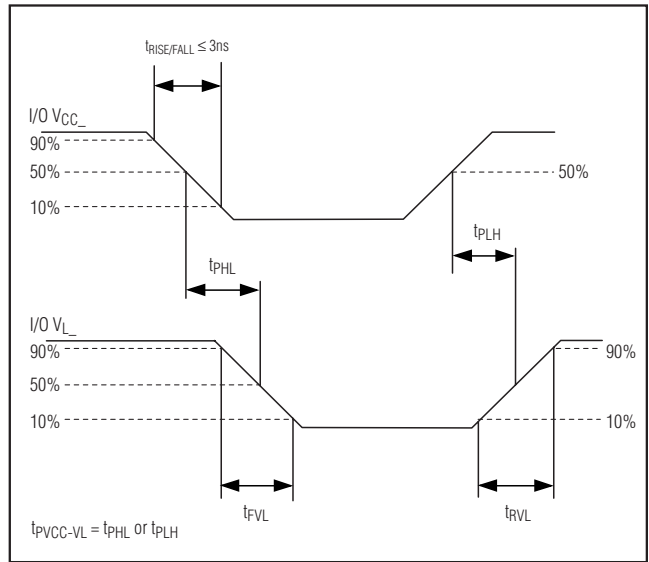


Figure 2b. Timing for Driving I/O VCC_

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Test Circuits/Timing Diagrams (continued)

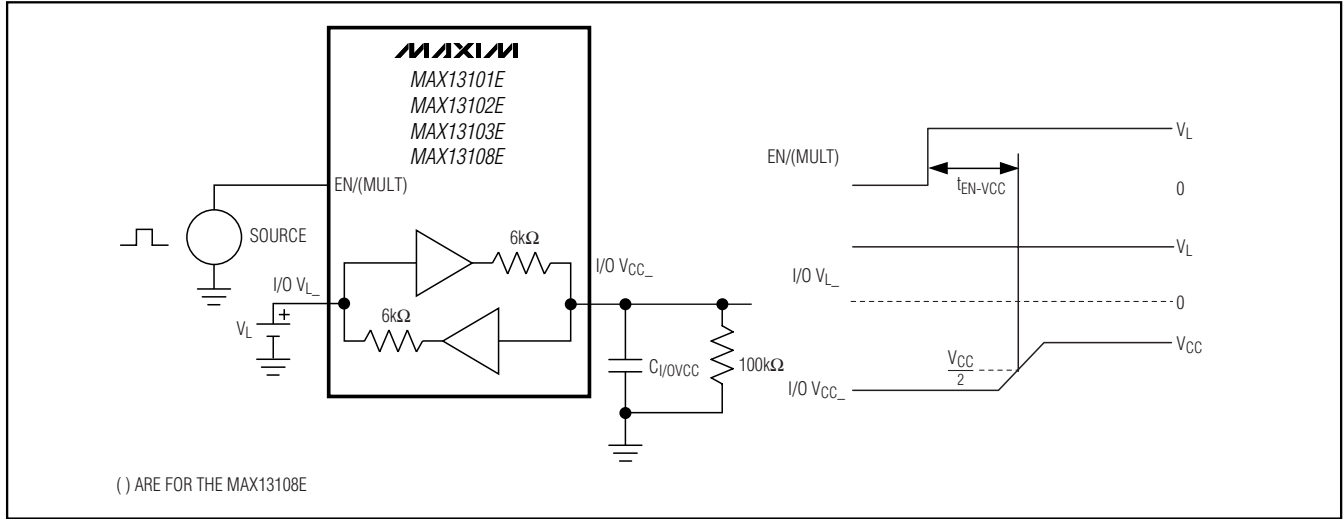


Figure 3. Propagation Delay from I/O VL₋ to I/O VCC₋ After EN

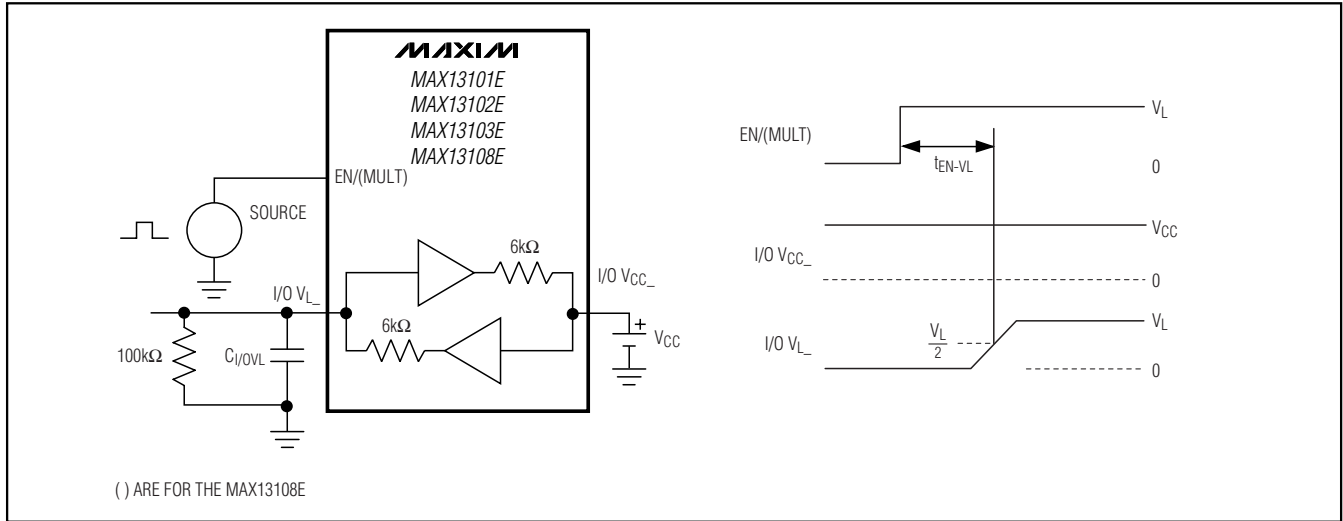
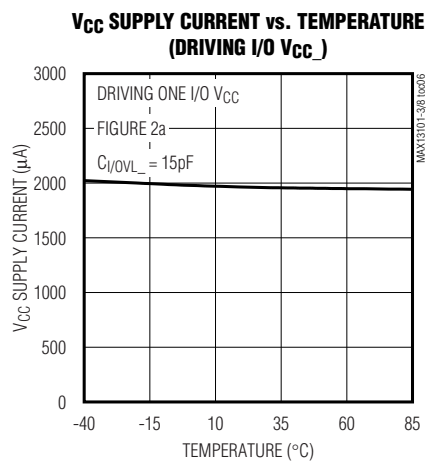
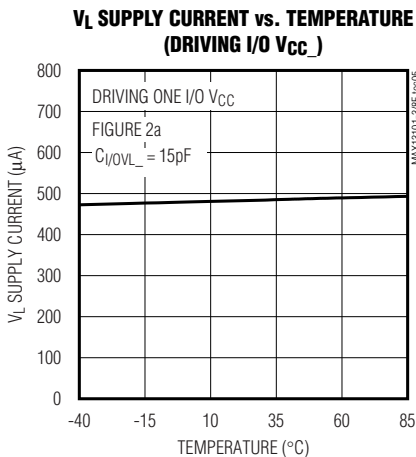
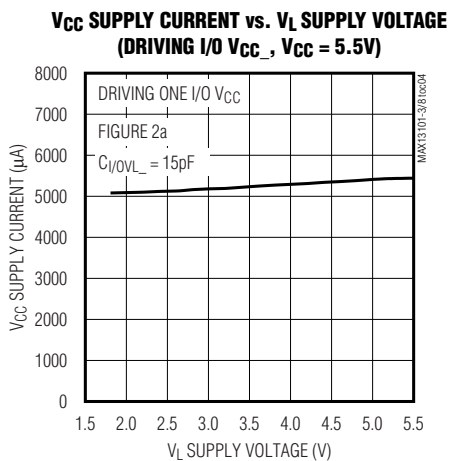
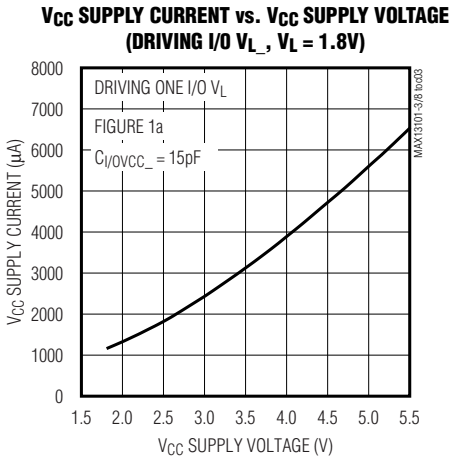
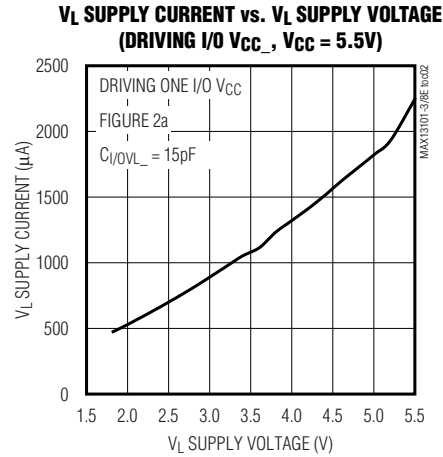
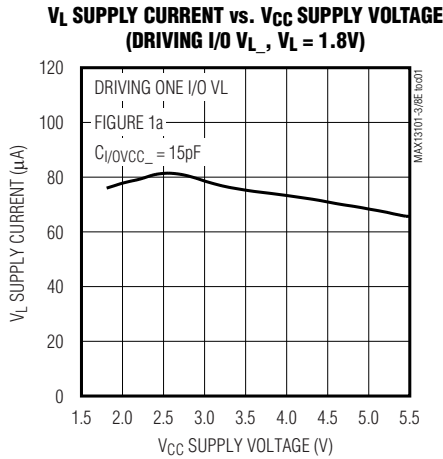


Figure 4. Propagation Delay from I/O VCC₋ to I/O VL₋ After EN

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Typical Operating Characteristics

($V_{CC} = 3.3V$, $V_L = 1.8V$, data rate = 20Mbps, $T_A = +25^\circ C$, unless otherwise noted.)

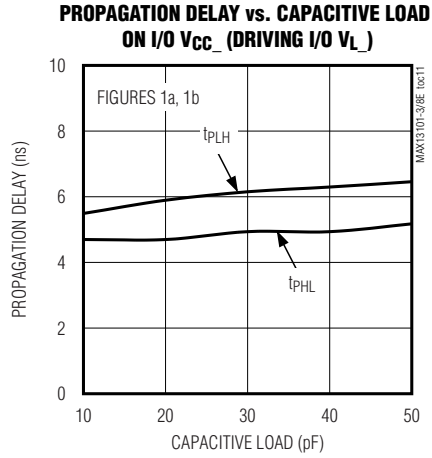
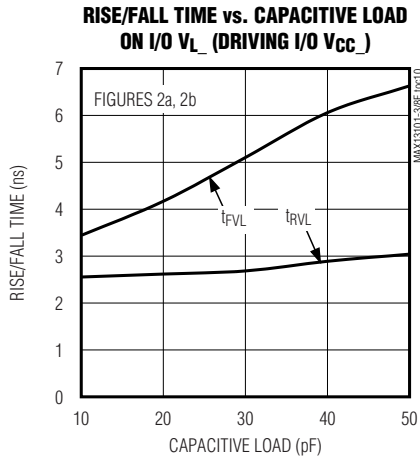
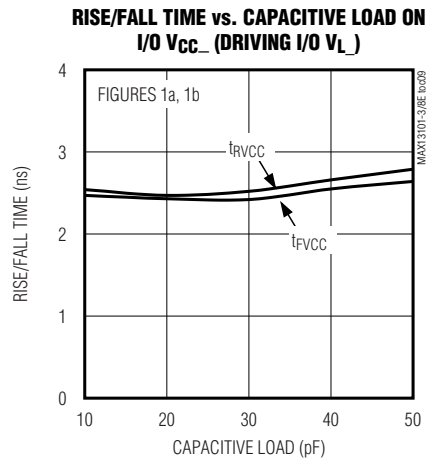
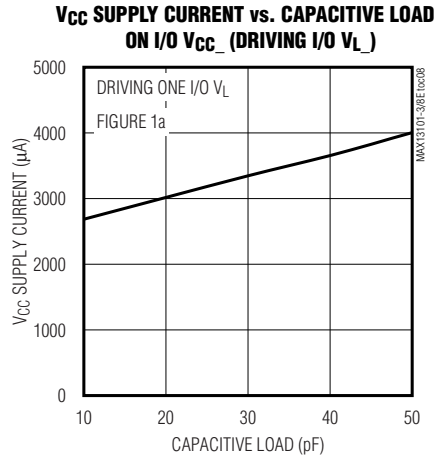
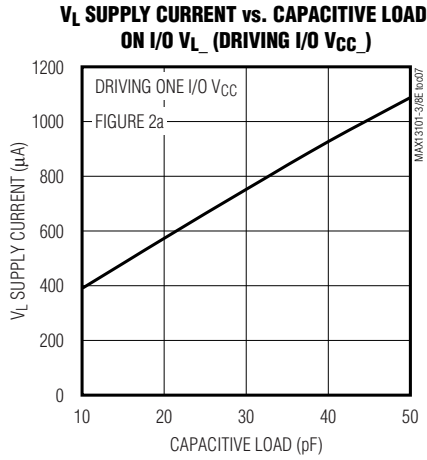


MAX13101E/MAX13102E/MAX13103E/MAX13108E

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Typical Operating Characteristics (continued)

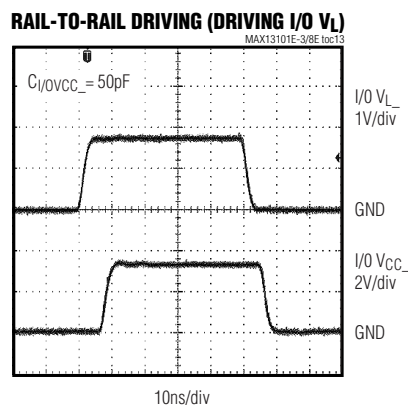
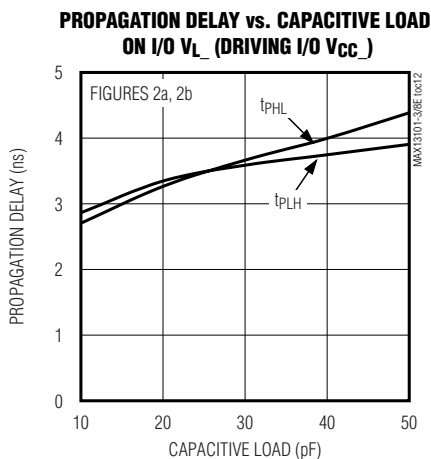
($V_{CC} = 3.3V$, $V_L = 1.8V$, data rate = 20Mbps, $T_A = +25^\circ C$, unless otherwise noted.)



16-Channel Buffered CMOS Logic-Level Translators

Typical Operating Characteristics (continued)

($V_{CC} = 3.3V$, $V_L = 1.8V$, data rate = 20Mbps, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description—MAX13101E/MAX13102E/MAX13103E

PIN		NAME	FUNCTION
TQFN	UCSP		
1, 21, 30	D6	GND	Ground
2	C2	I/O V_L5	Input/Output 5. Referenced to V_L .
3	A3	I/O V_L6	Input/Output 6. Referenced to V_L .
4	B3	I/O V_L7	Input/Output 7. Referenced to V_L .
5	C3	I/O V_L8	Input/Output 8. Referenced to V_L .
6	A4	I/O V_L9	Input/Output 9. Referenced to V_L .
7	B4	I/O V_L10	Input/Output 10. Referenced to V_L .
8	C4	I/O V_L11	Input/Output 11. Referenced to V_L .
9	A5	I/O V_L12	Input/Output 12. Referenced to V_L .
10	C6	EN	Global Enable Input. Pull EN low for shutdown. Drive EN to V_{CC} or V_L for normal operation.
11	B5	I/O V_L13	Input/Output 13. Referenced to V_L .
12	C5	I/O V_L14	Input/Output 14. Referenced to V_L .
13	A6	I/O V_L15	Input/Output 15. Referenced to V_L .
14	B6	I/O V_L16	Input/Output 16. Referenced to V_L .
15, 36	A1	V_L	Logic Supply Voltage, $+1.2V \leq V_L \leq V_{CC}$. Bypass V_L to GND with a $0.1\mu F$ capacitor.
16, 35	F1	V_{CC}	V_{CC} Supply Voltage, $+1.65V \leq V_{CC} \leq +5.5V$. Bypass V_{CC} to GND with a $0.1\mu F$ capacitor. For full ESD protection, connect a $1.0\mu F$ capacitor from V_{CC} to GND, located as close to the V_{CC} input as possible.
17	E6	I/O $V_{CC}16$	Input/Output 16. Referenced to V_{CC} .
18	F6	I/O $V_{CC}15$	Input/Output 15. Referenced to V_{CC} .

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Pin Description—MAX13101E/MAX13102E/MAX13103E (continued)

PIN		NAME	FUNCTION
TQFN	UCSP		
19	D5	I/O V _{CC14}	Input/Output 14. Referenced to V _{CC} .
20	E5	I/O V _{CC13}	Input/Output 13. Referenced to V _{CC} .
22	F5	I/O V _{CC12}	Input/Output 12. Referenced to V _{CC} .
23	D4	I/O V _{CC11}	Input/Output 11. Referenced to V _{CC} .
24	E4	I/O V _{CC10}	Input/Output 10. Referenced to V _{CC} .
25	F4	I/O V _{CC9}	Input/Output 9. Referenced to V _{CC} .
26	D3	I/O V _{CC8}	Input/Output 8. Referenced to V _{CC} .
27	E3	I/O V _{CC7}	Input/Output 7. Referenced to V _{CC} .
28	F3	I/O V _{CC6}	Input/Output 6. Referenced to V _{CC} .
29	D2	I/O V _{CC5}	Input/Output 5. Referenced to V _{CC} .
31	E2	I/O V _{CC4}	Input/Output 4. Referenced to V _{CC} .
32	F2	I/O V _{CC3}	Input/Output 3. Referenced to V _{CC} .
33	D1	I/O V _{CC2}	Input/Output 2. Referenced to V _{CC} .
34	E1	I/O V _{CC1}	Input/Output 1. Referenced to V _{CC} .
37	B1	I/O V _{L1}	Input/Output 1. Referenced to V _L .
38	C1	I/O V _{L2}	Input/Output 2. Referenced to V _L .
39	A2	I/O V _{L3}	Input/Output 3. Referenced to V _L .
40	B2	I/O V _{L4}	Input/Output 4. Referenced to V _L .
EP	—	EP	Exposed Paddle. Connect EP to GND.

Pin Description—MAX13108E

PIN		NAME	FUNCTION
TQFN	UCSP		
1, 21, 30	D6	GND	Ground
2	C2	I/O V _{L5}	Input/Output 5. Referenced to V _L .
3	A3	I/O V _{L6}	Input/Output 6. Referenced to V _L .
4	B3	I/O V _{L7}	Input/Output 7. Referenced to V _L .
5	C3	I/O V _{L8}	Input/Output 8. Referenced to V _L .
6	A4	I/O V _{L9}	Input/Output 9. Referenced to V _L .
7	B4	I/O V _{L10}	Input/Output 10. Referenced to V _L .
8	C4	I/O V _{L11}	Input/Output 11. Referenced to V _L .
9	A5	I/O V _{L12}	Input/Output 12. Referenced to V _L .

16-Channel Buffered CMOS Logic-Level Translators

Pin Description—MAX13108E (continued)

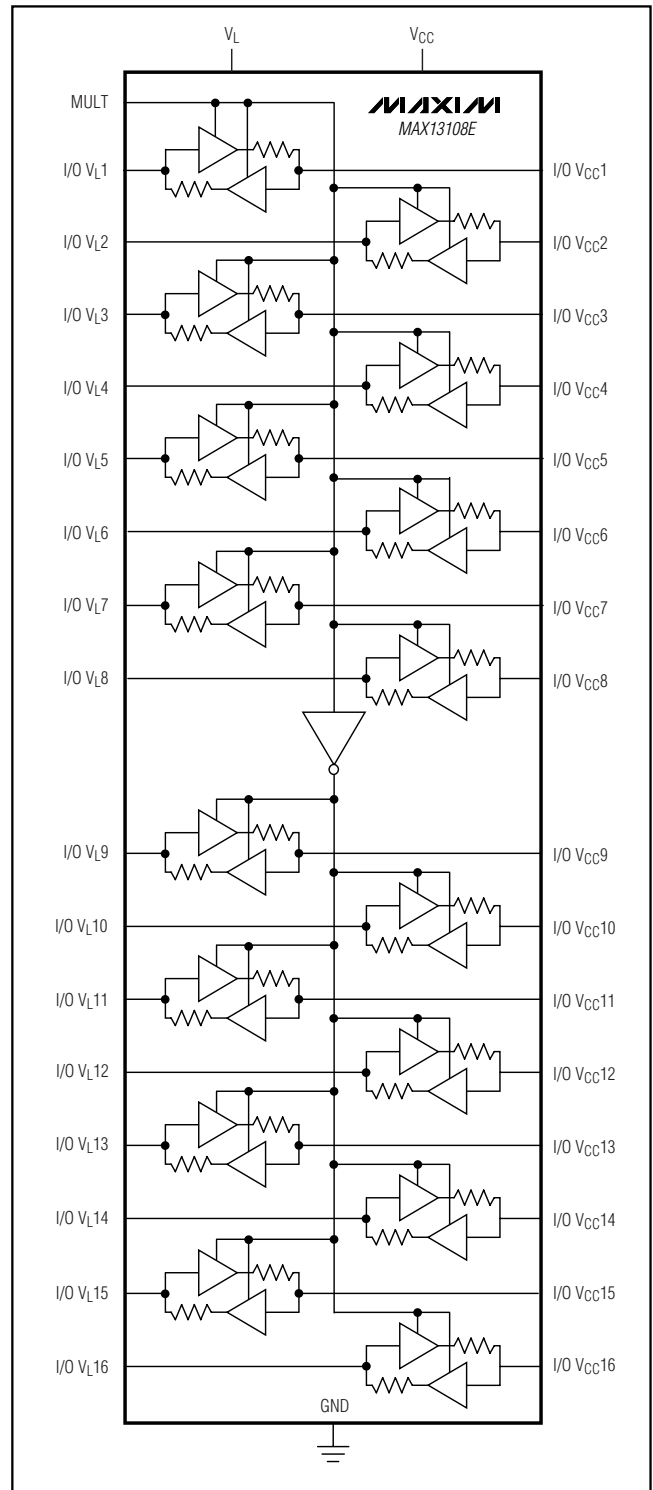
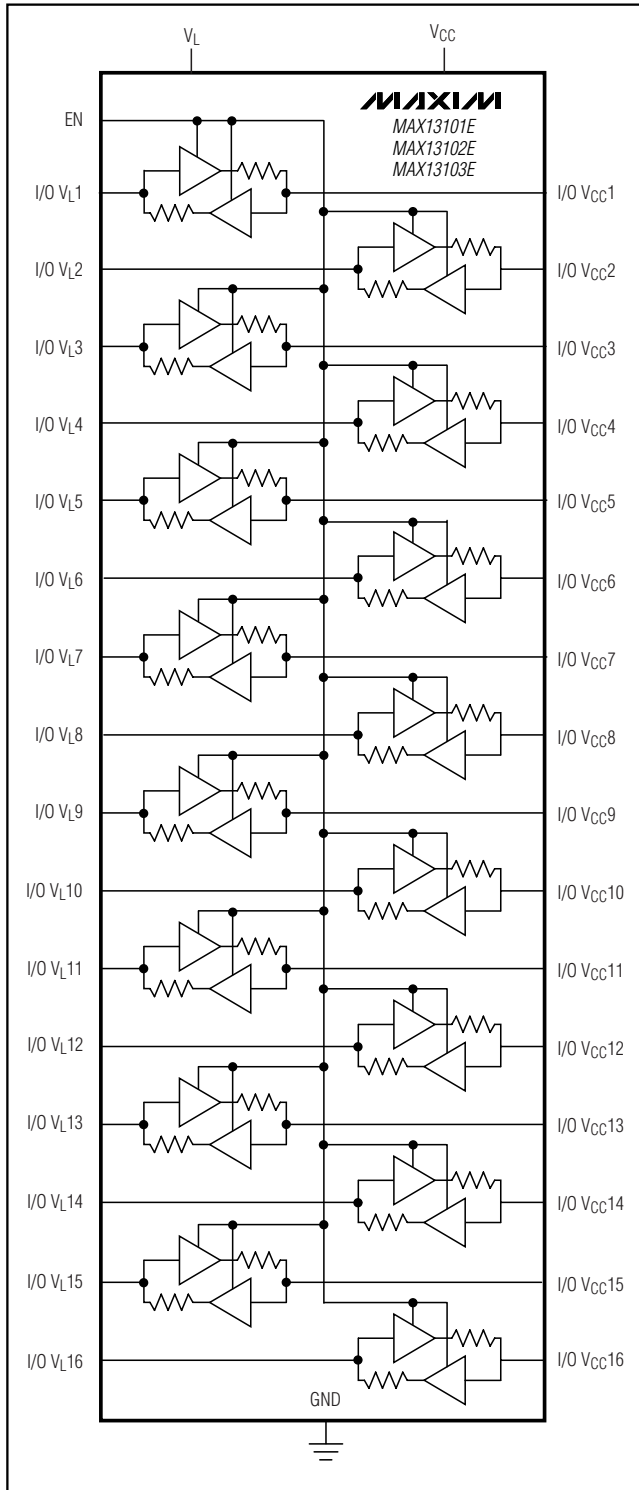
PIN		NAME	FUNCTION
TQFN	UCSP		
10	C6	MULT	Multiplexing Input. Drive MULT low to enable channels 9 to 16. Driving MULT low puts channels 1 to 8 into tri-state. Drive MULT to V _{CC} or V _L to enable channels 1 to 8. Driving MULT to V _{CC} or V _L puts channels 9 to 16 into tri-state.
11	B5	I/O V _L 13	Input/Output 13. Referenced to V _L .
12	C5	I/O V _L 14	Input/Output 14. Referenced to V _L .
13	A6	I/O V _L 15	Input/Output 15. Referenced to V _L .
14	B6	I/O V _L 16	Input/Output 16. Referenced to V _L .
15, 36	A1	V _L	Logic Supply Voltage, +1.2V ≤ V _L ≤ V _{CC} . Bypass V _L to GND with a 0.1μF capacitor.
16, 35	F1	V _{CC}	V _{CC} Supply Voltage, +1.65V ≤ V _{CC} ≤ +5.5V. Bypass V _{CC} to GND with a 0.1μF capacitor. For full ESD protection, connect a 1.0μF capacitor from V _{CC} to GND, located as close to the V _{CC} input as possible.
17	E6	I/O V _{CC} 16	Input/Output 16. Referenced to V _{CC} .
18	F6	I/O V _{CC} 15	Input/Output 15. Referenced to V _{CC} .
19	D5	I/O V _{CC} 14	Input/Output 14. Referenced to V _{CC} .
20	E5	I/O V _{CC} 13	Input/Output 13. Referenced to V _{CC} .
22	F5	I/O V _{CC} 12	Input/Output 12. Referenced to V _{CC} .
23	D4	I/O V _{CC} 11	Input/Output 11. Referenced to V _{CC} .
24	E4	I/O V _{CC} 10	Input/Output 10. Referenced to V _{CC} .
25	F4	I/O V _{CC} 9	Input/Output 9. Referenced to V _{CC} .
26	D3	I/O V _{CC} 8	Input/Output 8. Referenced to V _{CC} .
27	E3	I/O V _{CC} 7	Input/Output 7. Referenced to V _{CC} .
28	F3	I/O V _{CC} 6	Input/Output 6. Referenced to V _{CC} .
29	D2	I/O V _{CC} 5	Input/Output 5. Referenced to V _{CC} .
31	E2	I/O V _{CC} 4	Input/Output 4. Referenced to V _{CC} .
32	F2	I/O V _{CC} 3	Input/Output 3. Referenced to V _{CC} .
33	D1	I/O V _{CC} 2	Input/Output 2. Referenced to V _{CC} .
34	E1	I/O V _{CC} 1	Input/Output 1. Referenced to V _{CC} .
37	B1	I/O V _L 1	Input/Output 1. Referenced to V _L .
38	C1	I/O V _L 2	Input/Output 2. Referenced to V _L .
39	A2	I/O V _L 3	Input/Output 3. Referenced to V _L .
40	B2	I/O V _L 4	Input/Output 4. Referenced to V _L .
EP	—	EP	Exposed Paddle. Connect EP to GND.

MAX13101E/MAX13102E/MAX13103E/MAX13108E

16-Channel Buffered CMOS Logic-Level Translators

MAX13101E/MAX13102E/MAX13103E/MAX13108E

Functional Diagrams



16-Channel Buffered CMOS Logic-Level Translators

Detailed Description

The MAX13101E/MAX13102E/MAX13103E/MAX13108E logic-level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L , set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX13101E/MAX13102E/MAX13103E/MAX13108E are bidirectional level translators allowing data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX13101E/MAX13102E/MAX13103E/MAX13108E accept V_L from +1.2V to V_{CC} . All devices have a V_{CC} range from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13101E/MAX13102E/MAX13103E feature an output enable mode that reduces V_{CC} supply current to less than $1\mu\text{A}$, and V_L supply current to less than $2\mu\text{A}$ when in shutdown. The MAX13108E features a multiplexing input that selects one byte between the two, thus allowing multiplexing of the signals. The MAX13101E/MAX13102E/MAX13103E/MAX13108E have $\pm 15\text{kV}$ ESD protection on the I/O V_{CC} side for greater protection in applications that route signals externally. The MAX13101E/MAX13102E/MAX13103E/MAX13108E operate at a guaranteed data rate of 20Mbps. The maximum data rate depends heavily on the load capacitance (see the *Typical Operating Characteristics*) and the output impedance of the external driver.

Power-Supply Sequencing

For proper operation, ensure that $+1.65\text{V} \leq V_{CC} \leq +5.5\text{V}$, $+1.2\text{V} \leq V_L \leq +5.5\text{V}$, and $V_L \leq V_{CC}$. During power-up sequencing, $V_L \geq V_{CC}$ does not damage the device. When V_{CC} is disconnected and V_L is powering up, up to 10mA of current can be sourced to each load on the V_L side, yet the device does not latch up. To guarantee that no excess leakage current flows and that the device does not interfere with the I/O on the V_L side, V_{CC} should be connected to GND with a max 50Ω resistor when the V_{CC} supply is not present (Figure 5).

Input Driver Requirements

The MAX13101E/MAX13102E/MAX13103E/MAX13108E architecture is based on a one-shot accelerator output stage (Figure 6). Accelerator output stages are always in tri-state except when there is a transition on any of the translators on the input side, either I/O $V_{L_}$ or I/O $V_{CC_}$. Then a short pulse is generated, during which the accelerator output stages become active and charge/discharge the capacitances at the I/Os. Due to

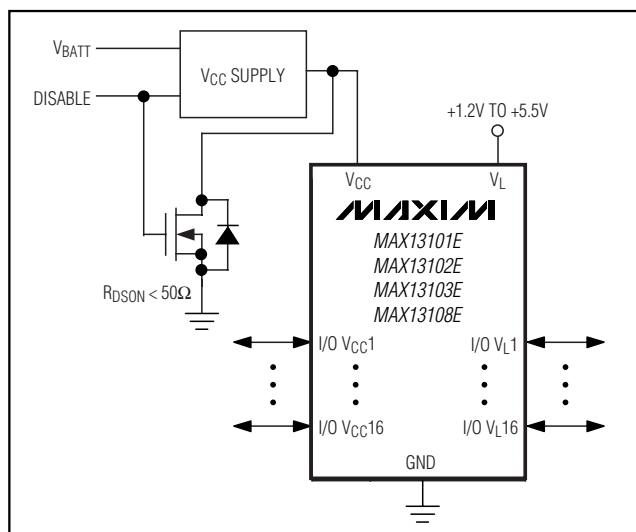


Figure 5. Recommended Circuit for Powering Down V_{CC}

the bidirectional nature, both input stages become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

For proper full-speed operation, the output current of a device that drives the inputs of the MAX13101E/MAX13102E/MAX13103E/MAX13108E should meet the following requirement:

$$i > 10^8 \times V \times (C + 10\text{pF})$$

where, i is the driver output current, V is the logic-supply voltage (i.e., V_L or V_{CC}) and C is the parasitic capacitance of the signal line.

Enable Output Mode (EN)

The MAX13101E/MAX13102E/MAX13103E feature an enable input (EN) that, when driven low, places the device into shutdown mode. During shutdown, the MAX13101E I/O $V_{CC_}$ ports are pulled down to ground with internal $6\text{k}\Omega$ resistors and the I/O $V_{L_}$ ports enter tri-state. MAX13102E I/O $V_{CC_}$ lines enter tri-state and the I/O $V_{L_}$ lines are pulled down to ground with internal $6\text{k}\Omega$ resistors. All I/O $V_{CC_}$ and I/O $V_{L_}$ lines on the MAX13103E enter tri-state while the device is in shutdown mode. During shutdown, the V_{CC} supply current reduces to less than $1\mu\text{A}$, and the V_L supply current reduces to less than $2\mu\text{A}$. To guarantee minimum shutdown supply current, all I/O $V_{L_}$ need to be driven to GND or V_L , or pulled to GND or V_L through $100\text{k}\Omega$ resistors. All I/O $V_{CC_}$ need to be driven to GND or V_{CC} , or pulled to GND or V_{CC} through $100\text{k}\Omega$ resistors. Drive EN to logic-high (V_L or V_{CC}) for normal operation.

MAX13101E/MAX13102E/MAX13103E/MAX13108E

16-Channel Buffered CMOS Logic-Level Translators

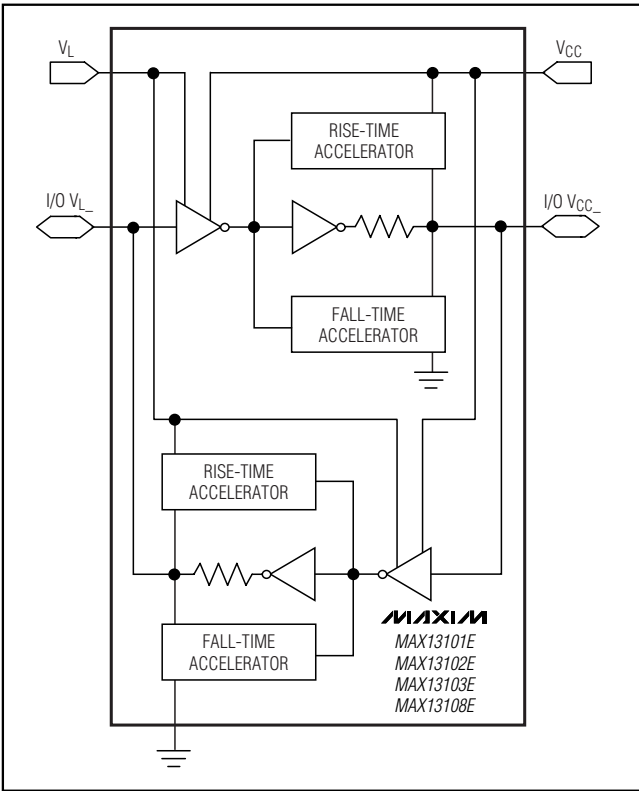


Figure 6. Simplified Diagram (1 I/O Line)

Multiplexing Input (MULT)

The MAX13108E features a multiplexing input (MULT) that enables 8 of the 16 channels and places the remaining 8 into tri-state. Figure 7 depicts a typical multiplexing configuration using the MAX13108E. Drive MULT high to enable I/O $V_{CC}1$ through I/O $V_{CC}8$ and I/O V_L1 through I/O V_L8 . Driving MULT high sets I/O $V_{CC}9$ through I/O $V_{CC}16$ and I/O V_L9 through I/O V_L16 into tri-state. Drive MULT low to enable I/O $V_{CC}9$ through I/O $V_{CC}16$ and I/O V_L9 through I/O V_L16 . Driving MULT low sets I/O $V_{CC}1$ through I/O $V_{CC}8$ and I/O V_L1 through I/O V_L8 into tri-state.

$\pm 15kV$ ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O V_{CC} lines have extra protection against static discharge. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of $\pm 15kV$ without damage. The ESD structures withstand high ESD in all states: normal operation, tri-state output mode, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing products can latch and must be powered down to remove the latchup condition.

ESD protection can be tested in various ways. The I/O V_{CC} lines of the MAX13101E/ MAX13102E/ MAX13103E/MAX13108E are characterized for protection to $\pm 15kV$ using the Human Body Model.

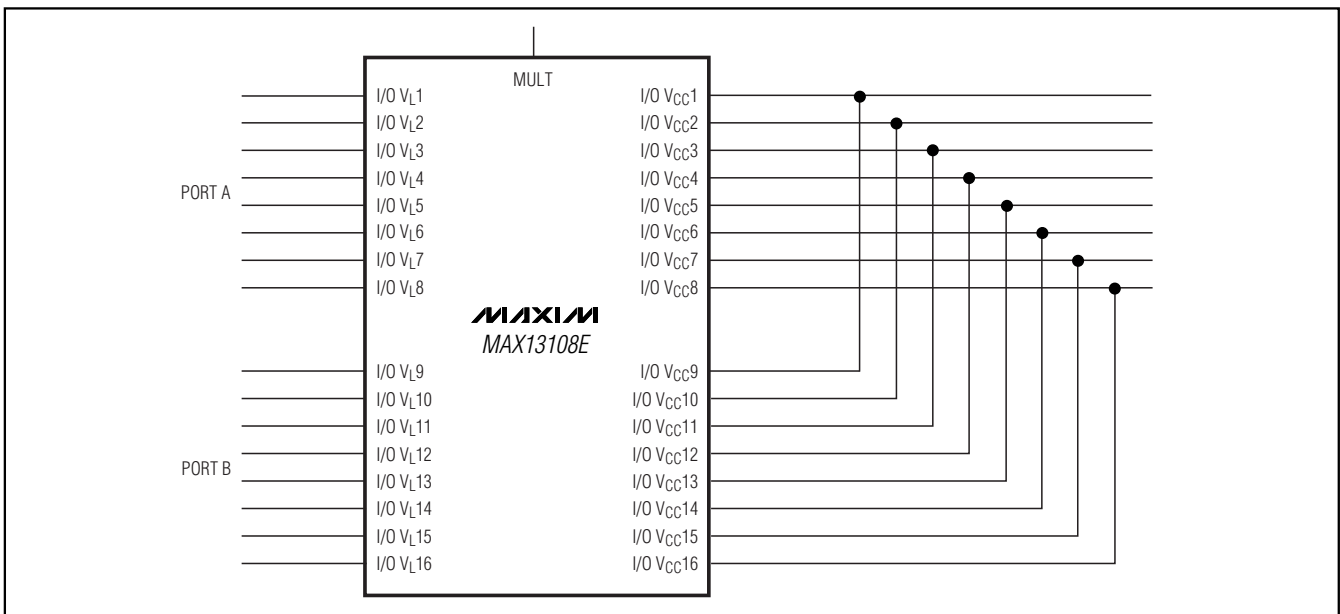


Figure 7. MAX13108E Multiplexing Configuration

16-Channel Buffered CMOS Logic-Level Translators

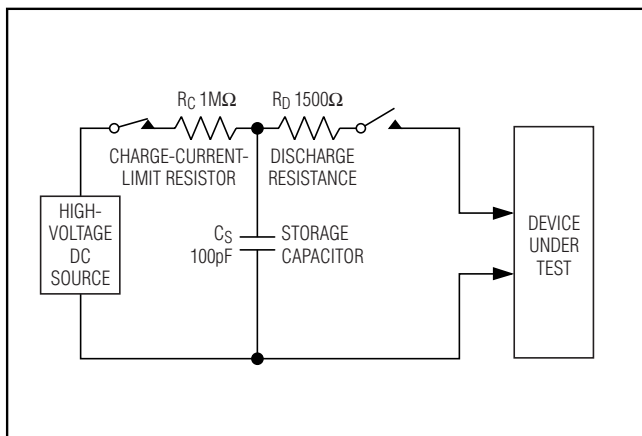


Figure 8a. Human Body ESD Test Model

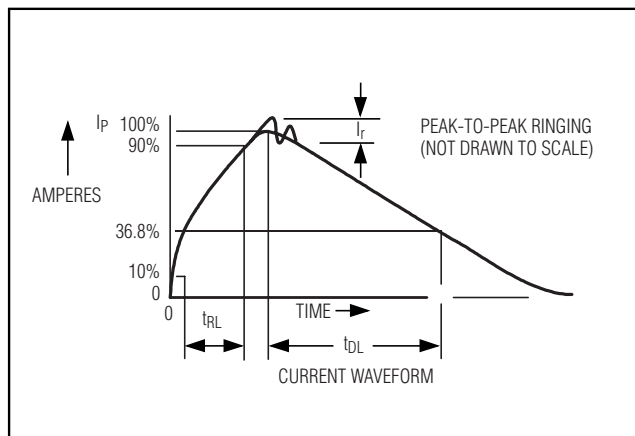


Figure 8b. Human Body Model Current Waveform

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 8a shows the Human Body Model and Figure 8b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with 0.1μF capacitors. To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1μF ceramic capacitor. Place all capacitors as close to the power-supply inputs as possible.

Capacitive Loading

Capacitive loading on the I/O lines impacts the rise time (and fall time) of the MAX13101E/MAX13102E/MAX13103E/MAX13108E when driving the signal lines. The actual rise time is a function of the parasitic capacitance, the supply voltage, and the drive impedance of the MAX13101E/MAX13102E/MAX13103E/MAX13108E. For proper operation, the signal must reach the V_{OH} as required before the rise-time accelerators turn off.

MAX13101E/MAX13102E/MAX13103E/MAX13108E

16-Channel Buffered CMOS Logic-Level Translators

Ordering Information/Selector Guide (continued)

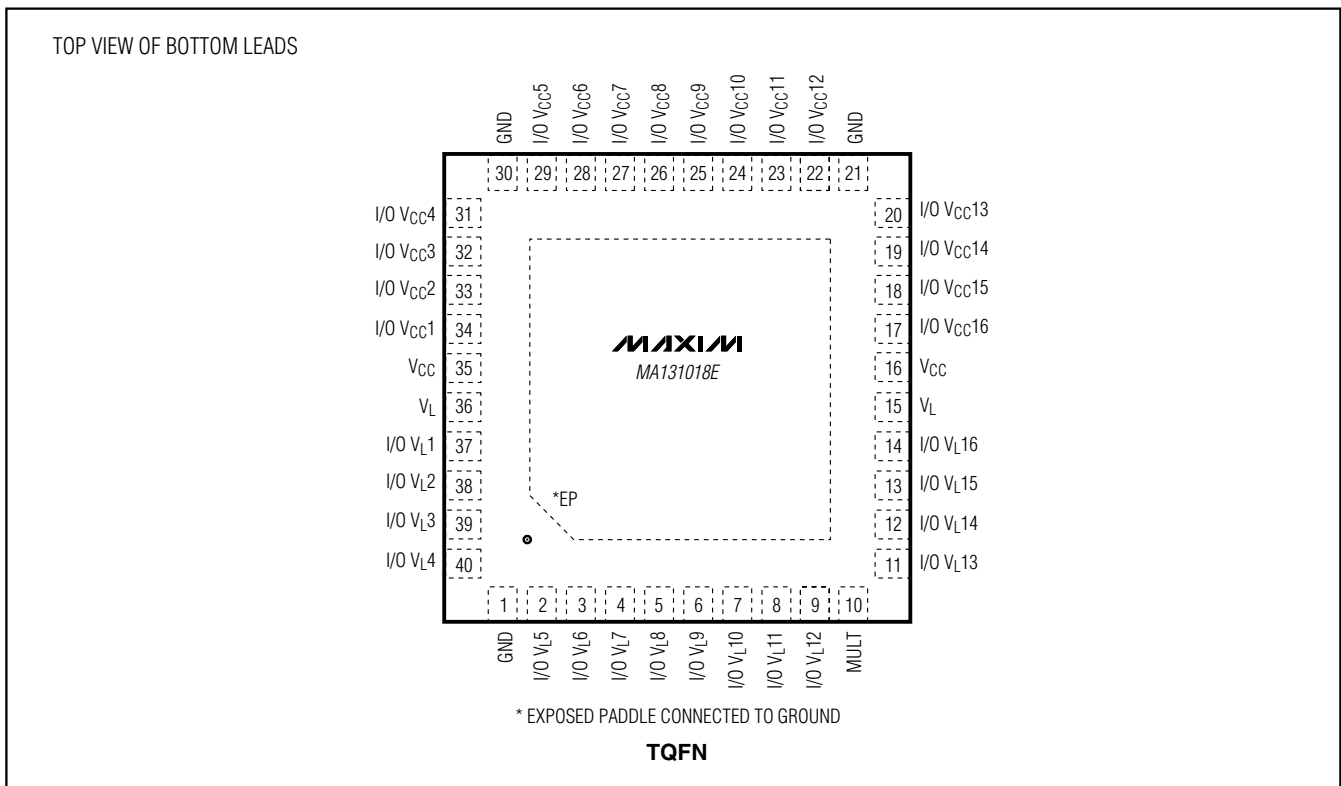
PART	PIN-PACKAGE	DATA RATE (Mbps)	I/O V _L STATE DURING SHUTDOWN	I/O V _{CC} STATE DURING SHUTDOWN	MULTIPLEXER FEATURE	PKG CODE
MAX13102EEBX*	36 UCSP** 3.06mm x 3.06mm	20	6kΩ to GND	High impedance	No	B36-1
MAX13102EETL	40 TQFN 5mm x 5mm x 0.8mm	20	6kΩ to GND	High impedance	No	T4055-1
MAX13103EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	High impedance	No	B36-1
MAX13103EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	High impedance	No	T4055-1
MAX13108EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	High impedance	Yes	B36-1
MAX13108EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	High impedance	Yes	T4055-1

Note: All devices operate over the -40°C to +85°C operating temperature range.

*Future Product—contact factory for availability.

**UCSP bumps are in a 6 x 6 array.

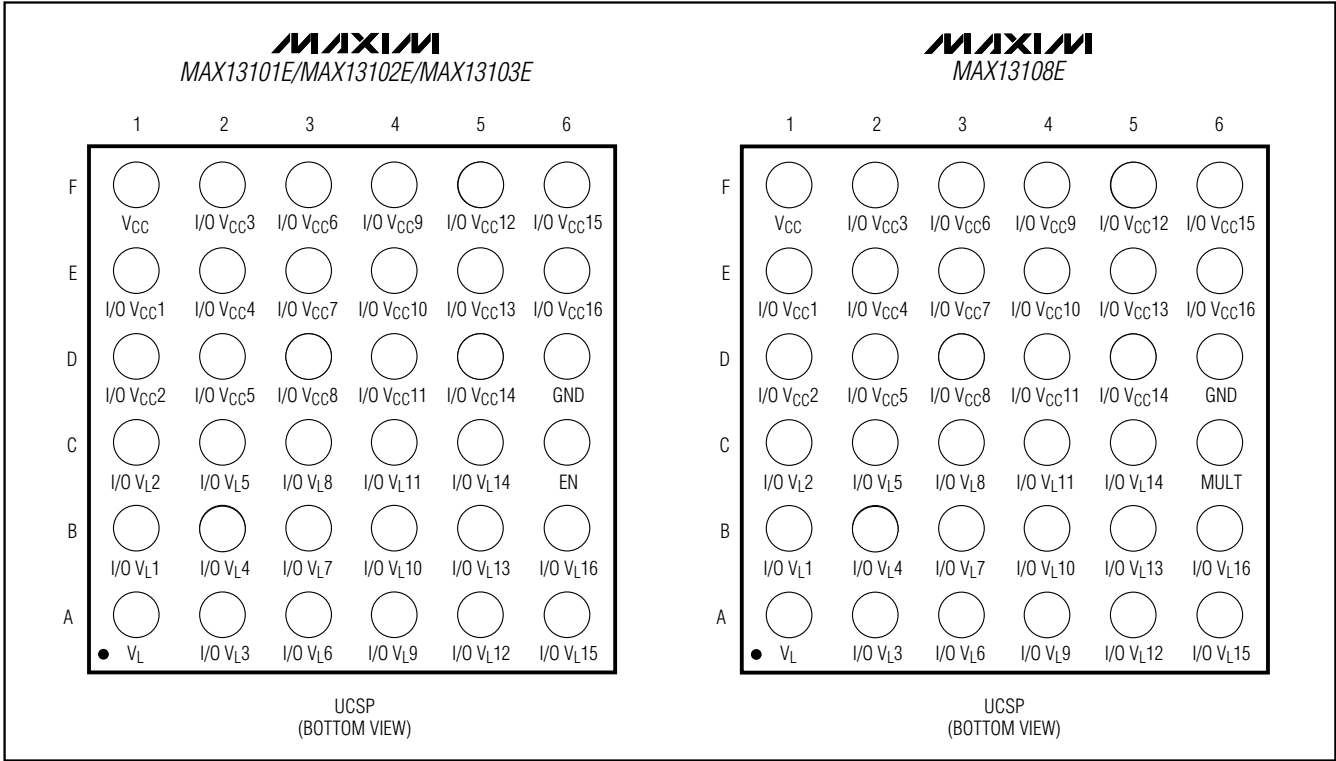
Pin Configurations (continued)



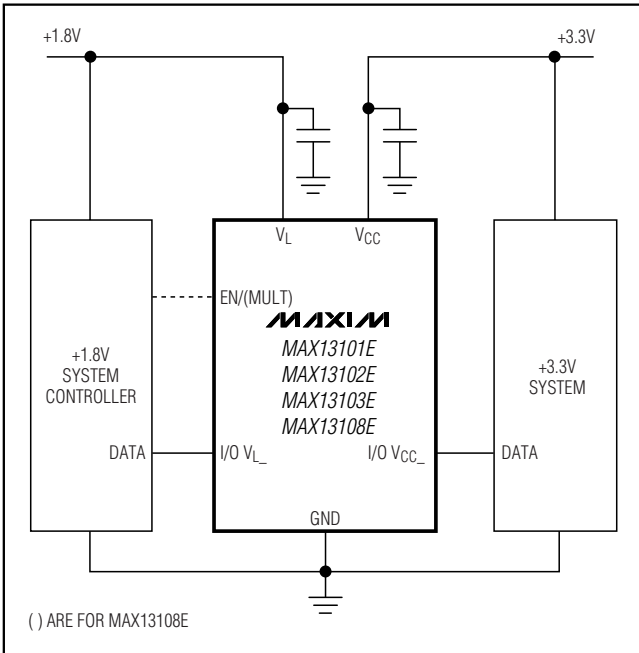
16-Channel Buffered CMOS Logic-Level Translators

Pin Configurations (continued)

MAX13101E/MAX13102E/MAX13103E/MAX13108E



Typical Operating Circuit



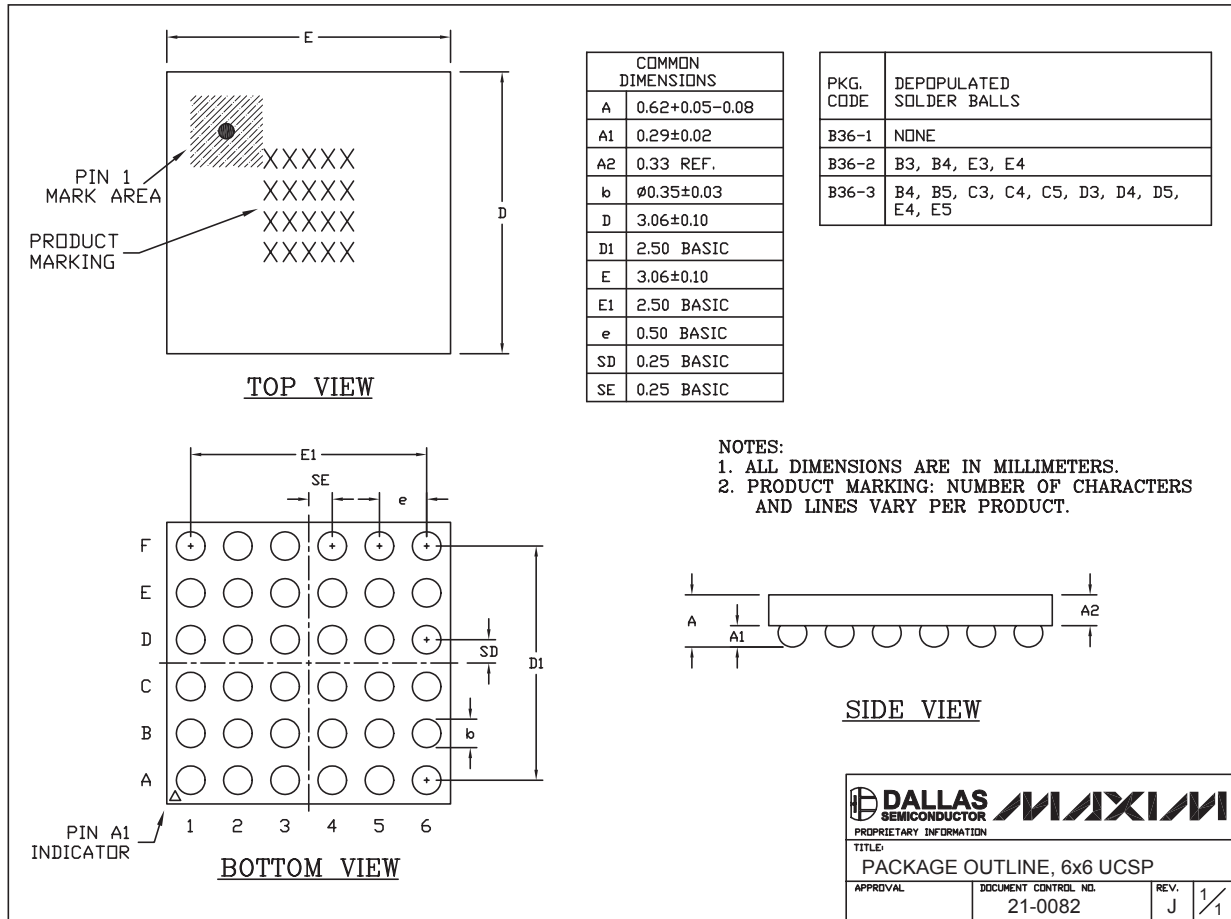
Chip Information

PROCESS: BICMOS

16-Channel Buffered CMOS Logic-Level Translators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

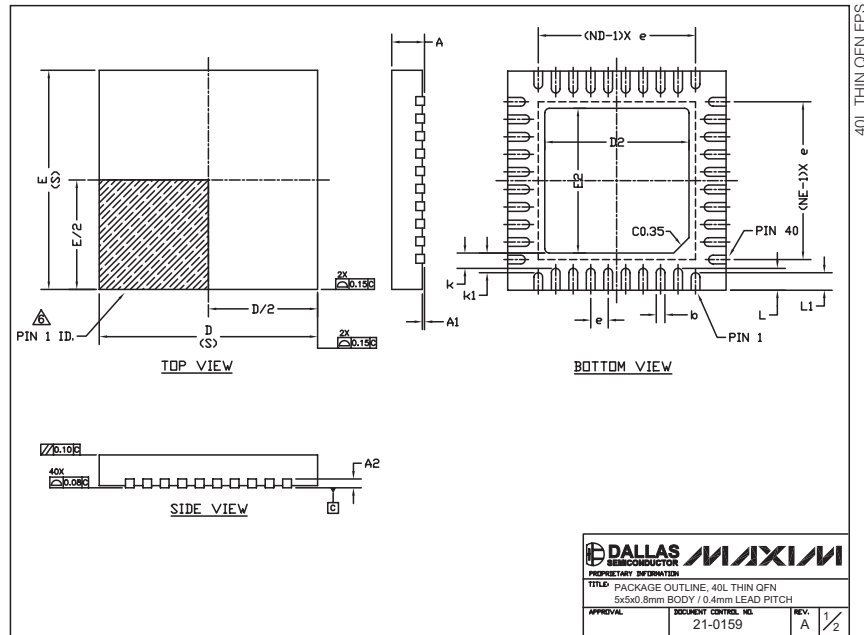


36L UCSP.EPS

16-Channel Buffered CMOS Logic-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
- WARPAGE SHALL NOT EXCEED 0.10mm.
- PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTICS. (S)
- REFER TO JEDEC MO-220.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

SYMBOLS	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.700	0.750	0.800
A1	0.000	--	0.050
A2	0.200 REF.		
b	0.150	0.200	0.250
D	4.900	5.000	5.100
e	0.400 TYP.		
E	4.900	5.000	5.100
k	0.250	0.350	0.450
k1	0.350	0.450	0.550
L	0.400	0.500	0.600
L1	0.300	0.400	0.500
N	40		
ND	10		
NE	10		

PKG. CODE	EXPOSED PAD VARIATIONS					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40

DALLAS SEMICONDUCTOR **MAXIM**
 PROPRIETARY INFORMATION
 TITLE: PACKAGE OUTLINE, 40L THIN QFN
 5x5x0.8mm BODY / 0.4mm LEAD PITCH
 APPROVAL: _____ DOCUMENT CONTROL NO. 21-0159 REV. A 1/2

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