TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM3401

30V P-Channel MOSFET

SOT-23

Pin Definition:
1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
-30	60 @ V_{GS} = 10V	3.0
	90 @ V_{GS} = 4.5V	2.0

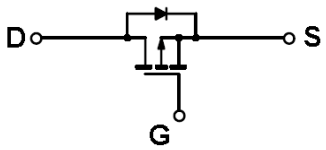
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM3401CX RF	SOT-23	T&R

Absolute Maximum Rating (Ta = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30V	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, V_{GS} @4.5V.		I_D	-3	A
Pulsed Drain Current, V_{GS} @4.5V		I_{DM}	-10	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	-1.9	A
Maximum Power Dissipation	Ta = 25 °C	P_D	1.25	W
	Ta = 70°C		0.8	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Foot (Drain) Thermal Resistance	$R\Theta_{JF}$	30	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	50	°C/W

Notes:

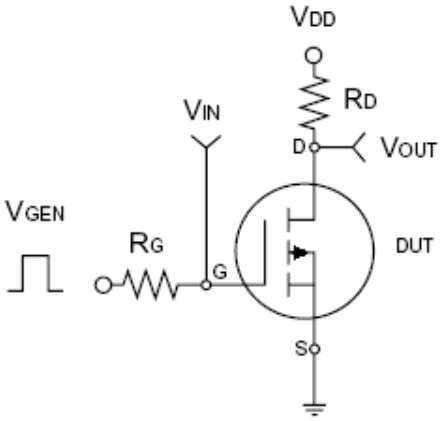
a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

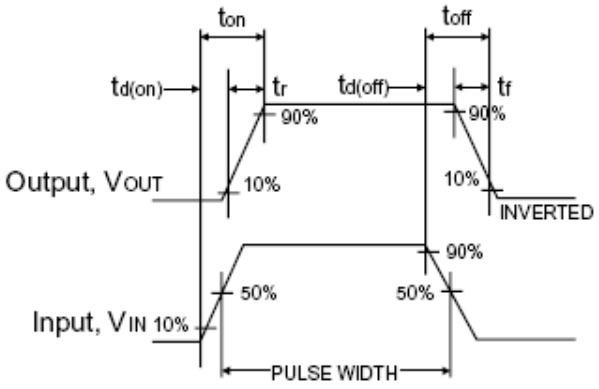
Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250uA	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	$V_{GS(TH)}$	-1.0	-1.5	-3.0	V
Gate Body Leakage	V_{GS} = ±24V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -20V, V_{GS} = 0V	I_{DSS}	--	--	-1.0	μA
On-State Drain Current[a]	V_{DS} =-5V, V_{GS} = -10V	$I_{D(ON)}$	-6	--	--	A
Drain-Source On-State Resistance[a]	V_{GS} = -4.5V, I_D = -2.0A	$R_{DS(ON)}$	--	75	90	mΩ
	V_{GS} = -10V, I_D = -3.0A		--	50	60	
Forward Transconductance[a]	V_{DS} = -15V, I_D = -5A	g_{fs}	4	7	--	S
Diode Forward Voltage	I_S = -1.9A, V_{GS} = 0V	V_{SD}	--	-0.8	-1.3	V
Dynamic[b]						
Total Gate Charge	V_{DS} = -15V, I_D = -3A, V_{GS} = -10V	Q_g	--	9.52		nC
Gate-Source Charge		Q_{gs}	--	3.43	--	
Gate-Drain Charge		Q_{gd}	--	1.71	--	
Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	551.57	--	pF
Output Capacitance		C_{oss}	--	90.96	--	
Reverse Transfer Capacitance		C_{rss}	--	60.79	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = -15V, R_L = 15Ω, I_D = -1A, V_{GEN} = -10V, R_G = 6Ω	$t_{d(on)}$	--	10.8	--	nS
Turn-On Rise Time		t_r	--	2.33	--	
Turn-Off Delay Time		$t_{d(off)}$	--	22.53	--	
Turn-Off Fall Time		t_f	--	3.87	--	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



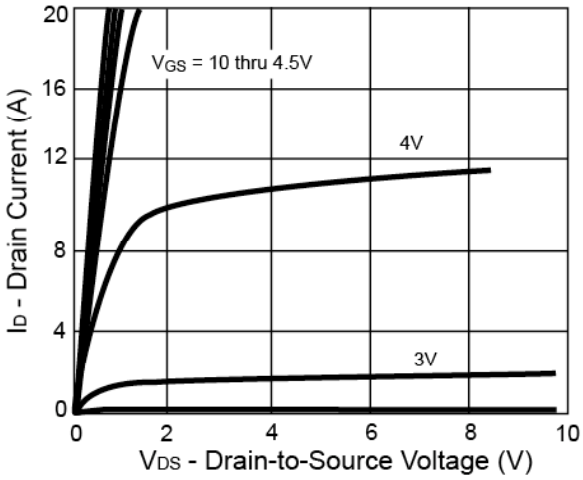
Switching Test Circuit



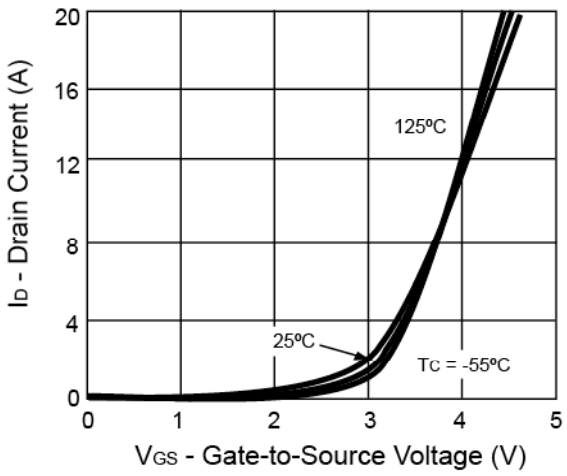
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

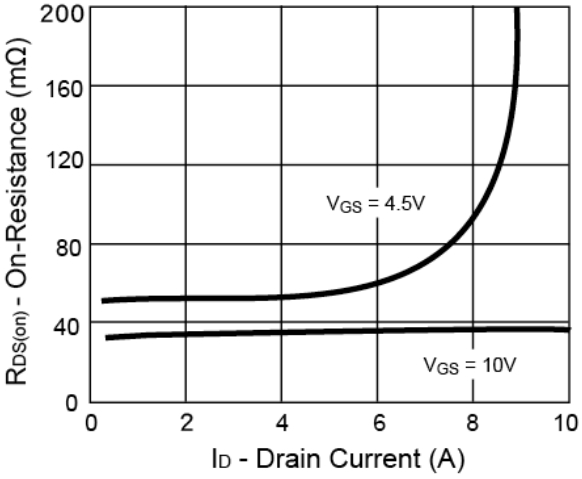
Output Characteristics



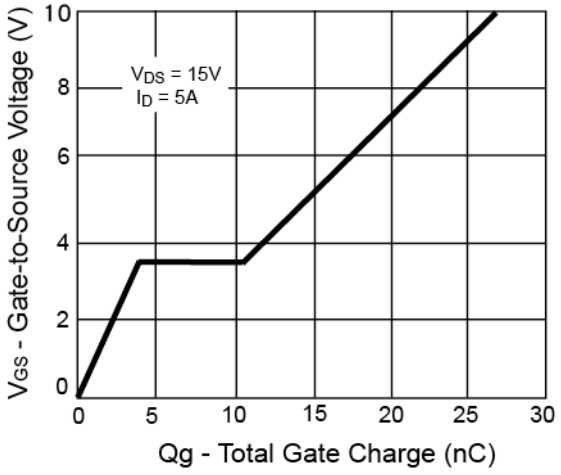
Transfer Characteristics



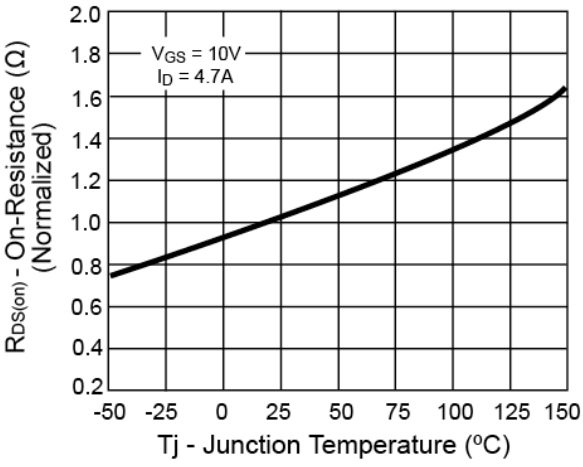
On-Resistance vs. Drain Current



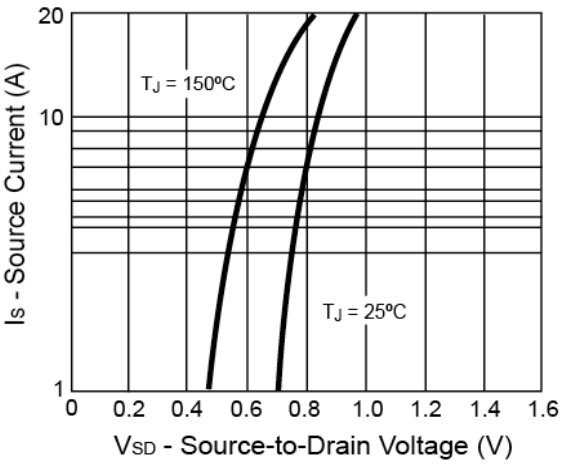
Gate Charge



On-Resistance vs. Junction Temperature

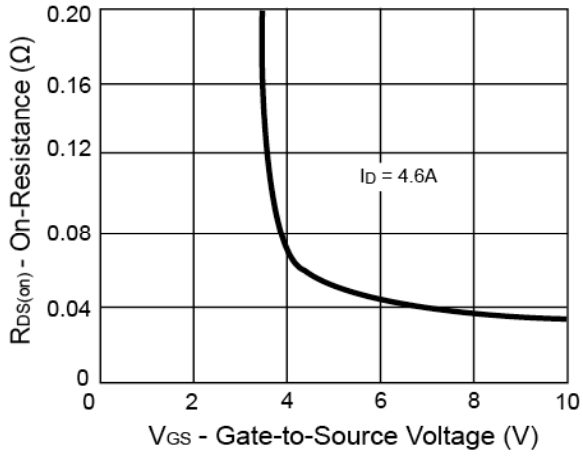


Source-Drain Diode Forward Voltage

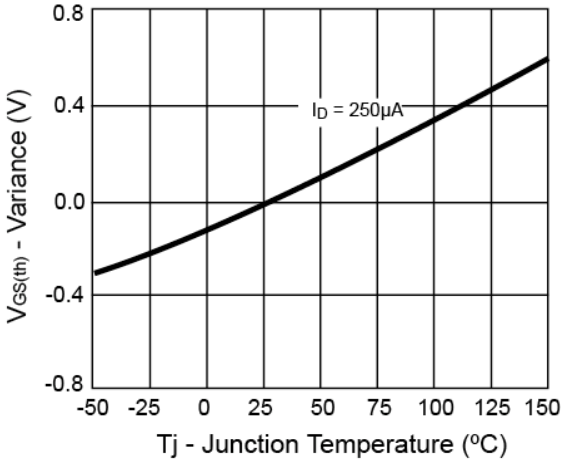


Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

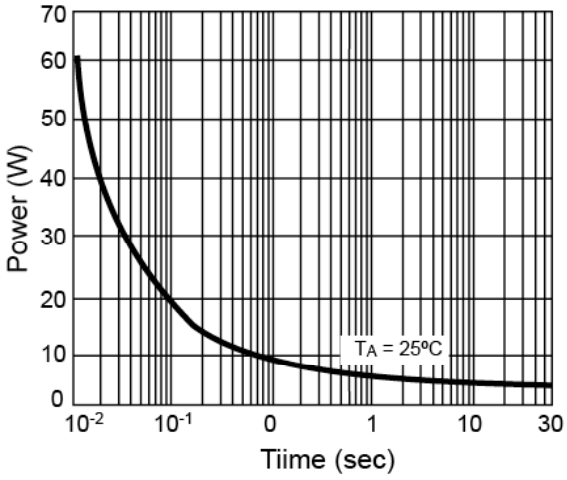
On-Resistance vs. Gate-Source Voltage



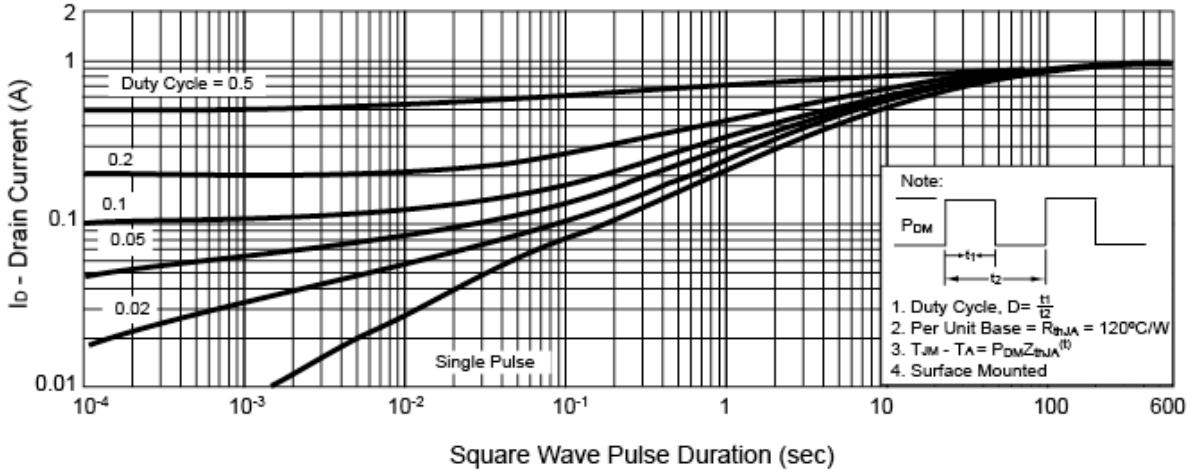
Threshold Voltage



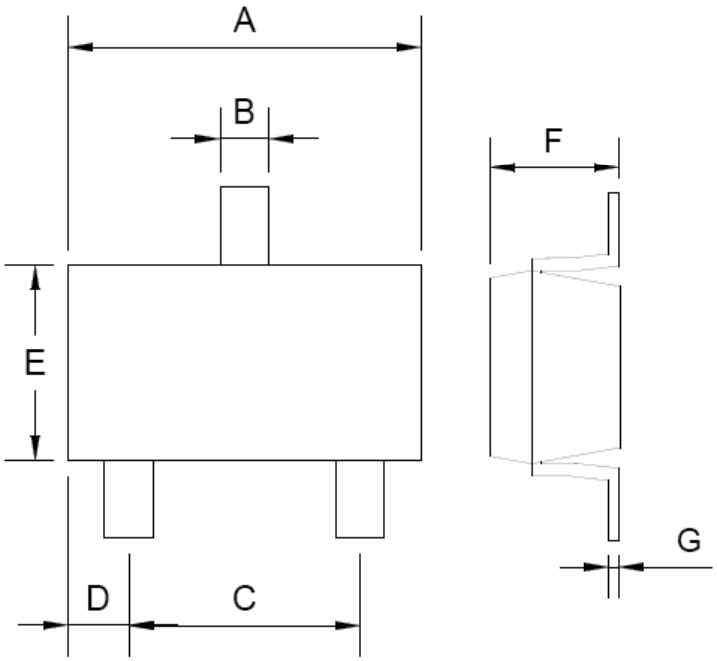
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Mechanical Drawing



SOT-23 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	2.88	2.91	0.113	0.115
B	0.39	0.42	0.015	0.017
C	1.78	2.03	0.070	0.080
D	0.51	0.61	0.020	0.024
E	1.59	1.66	0.063	0.065
F	1.04	1.08	0.041	0.043
G	0.07	0.09	0.003	0.004

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