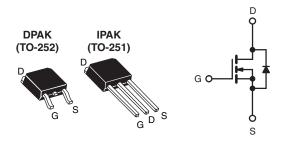


COMPLIANT

Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	500			
$R_{DS(on)}\left(\Omega\right)$	V _{GS} = 10 V	3.0		
Q _g (Max.) (nC)	19			
Q _{gs} (nC)	3.3			
Q _{gd} (nC)	13			
Configuration	Single			



N-Channel MOSFET

FEATURES

- · Dynamic dV/dt Rating
- · Repetitive Avalanche Rated
- Surface Mount (IRFR420, SiHFR420)
- Straight Lead (IRFU420, SiHFU420)
- · Available in Tape and Reel
- · Fast Switching
- · Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effictiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION						
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)	
Lead (Pb)-free	IRFR420PbF	IRFR420TRPbFa	IRFR420TRLPbFa	IRFR420TRRPbFa	IRFU420PbF	
	SiHFR420-E3	SiHFR420T-E3a	SiHFR420TL-E3a	-	SiHFU420-E3	
SnPb	IRFR420	IRFR420TRa	IRFR420TRL ^a	IRFR420TRR ^a	IRFU420	
SIIFD	SiHFR420	SiHFR420Ta	SiHFR420TL ^a	=	SiHFU420	

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS	Γ _C = 25 °C, u	nless otherw	vise noted			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	500	V	
Gate-Source Voltage			V _{GS}	± 20		
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	- I _D	2.4		
	V _{GS} at 10 V	$T_C = 25 \degree C$ $T_C = 100 \degree C$		1.5	Α	
Pulsed Drain Current ^a			I _{DM}	8.0	1	
Linear Derating Factor				0.33	W/°C	
Linear Derating Factor (PCB Mount)e				0.020	\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
Single Pulse Avalanche Energy ^b			E _{AS}	400	mJ	
Repetitive Avalanche Current ^a			I _{AR}	2.4	Α	
Repetitive Avalanche Energy ^a			E _{AR}	4.2	mJ	
Maximum Power Dissipation	T _C =	: 25 °C	٥	42	w	
Maximum Power Dissipation (PCB Mount)e	T _A =	25 °C	P_{D}	2.5	∀	
Peak Diode Recovery dV/dt ^c		dV/dt	3.5	V/ns		
Operating Junction and Storage Temperature Range			T _J , T _{stg} - 55 to + 150		°C	
Soldering Recommendations (Peak Temperature)	for 10 s		-	260 ^d		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD}=50~V$, starting $T_J=25~^{\circ}C$, L=124~mH, $R_g=25~\Omega$, $I_{AS}=2.4~A$ (see fig. 12). c. $I_{SD}\leq 2.4~A$, dl/dt $\leq 50~A/\mu s$, $V_{DD}\leq V_{DS}$, $T_J\leq 150~^{\circ}C$. d. 1.6 mm from case.

- e. When mounted on 1" square PCB (FR-4 or G-10 material).

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

IRFR420, IRFU420, SiHFR420, SiHFU420

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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	110		
Maximum Junction-to-Ambient (PCB Mount) ^a	R _{thJA}	-	50	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.0		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static				l			I
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	0.59	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	,	V _{GS} = ± 20 V		-	± 100	nA
Zava Cata Valtana Duain Courant	I _{DSS}	V _{DS} =	V _{DS} = 500 V, V _{GS} = 0 V		-	25	
Zero Gate Voltage Drain Current		V _{DS} = 400 V	', V _{GS} = 0 V, T _J = 125 °C	-	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D =1.4 A ^b	-	-	3.0	Ω
Forward Transconductance	9 _{fs}	V _{DS} :	= 50 V, I _D = 1.4 A	1.5	-	-	S
Dynamic							•
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0 MHz, see fig. 5		-	360	-	
Output Capacitance	C _{oss}			-	92	-	pF
Reverse Transfer Capacitance	C _{rss}			-	37	-	
Total Gate Charge	Qg			-	-	19	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 2.1 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 ^b		-	3.3	nC
Gate-Drain Charge	Q _{gd}	1			-	13	
Turn-On Delay Time	t _{d(on)}	$V_{DD}=250~V,~I_D=2.1~A,$ $R_g=18~\Omega,~R_D=120~\Omega,~see~fig.~10^b$		-	8.0	-	ns
Rise Time	t _r			-	8.6	-	
Turn-Off Delay Time	t _{d(off)}			-	33	-	
Fall Time	t _f			-	16	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	
Internal Source Inductance	L _S			-	7.5	-	- nH
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.4	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	8.0	A
Body Diode Voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 2.4 \text{A}, V_{GS} = 0 \text{V}^{\text{b}}$		-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	T - 25 °C 1	- 0 1 A dl/dt - 100 A/:-ch	-	260	520	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 2.1 \text{A}, dI/dt = 100 \text{A}/\mu\text{s}^{\text{b}}$		-	0.70	1.4	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	on is don	ninated b	v L _S and I	_D)	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300~\mu s$; duty cycle $\leq 2~\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

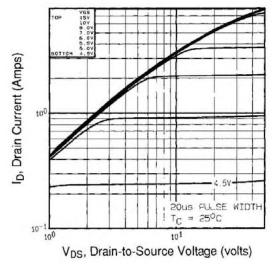


Fig. 1 - Typical Output Characteristics, $T_C = 25$ °C

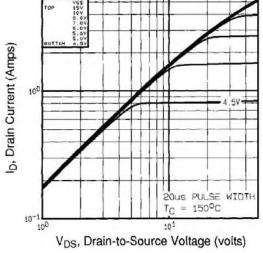


Fig. 2 -Typical Output Characteristics, T_C = 150 °C

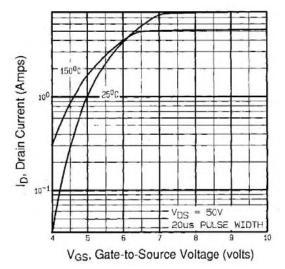


Fig. 3 - Typical Transfer Characteristics

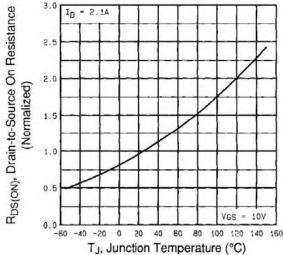


Fig. 4 - Normalized On-Resistance vs. Temperature

IRFR420, IRFU420, SiHFR420, SiHFU420

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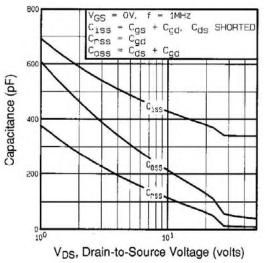


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

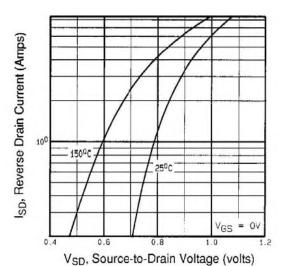


Fig. 7 - Typical Source-Drain Diode Forward Voltage

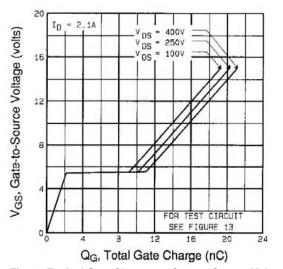


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

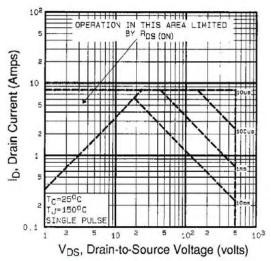


Fig. 8 - Maximum Safe Operating Area

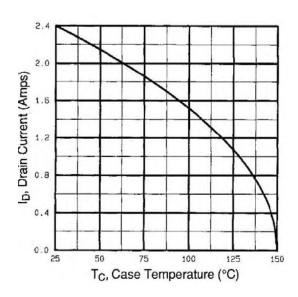


Fig. 9 - Maximum Drain Current vs. Case Temperature

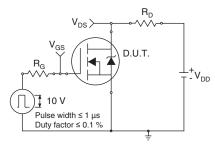


Fig. 10a - Switching Time Test Circuit

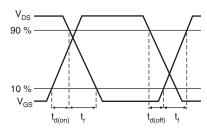


Fig. 10b - Switching Time Waveforms

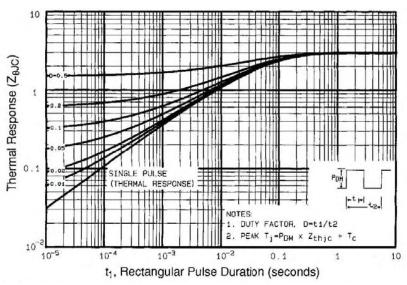


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

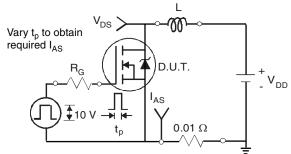


Fig. 12a - Unclamped Inductive Test Circuit

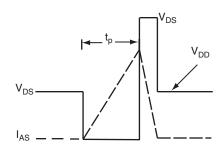


Fig. 12b - Unclamped Inductive Waveforms



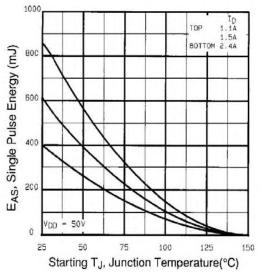


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

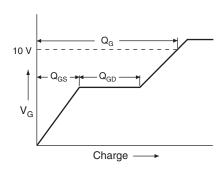


Fig. 13a - Basic Gate Charge Waveform

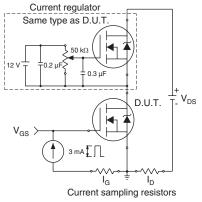
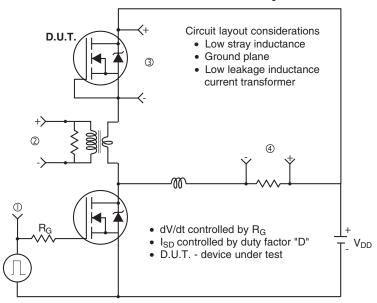
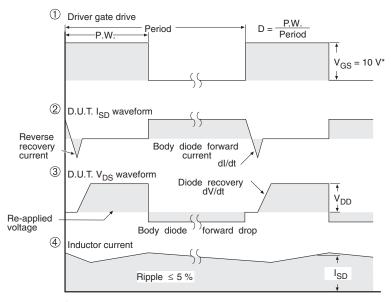


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices and 3 V drive devices

Fig. 14 -For N-Channel

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Revision: 18-Jul-08

Document Number: 91000 www.vishay.com