



P-Channel 100-V (D-S) MOSFET

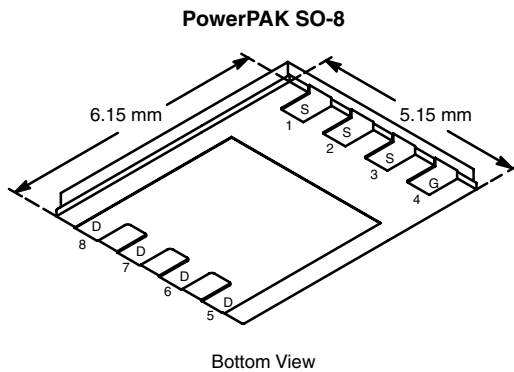
PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ)
- 100	0.041 at V _{GS} = - 10 V	- 28	54 nC
	0.047 at V _{GS} = - 4.5 V	- 28	

FEATURES

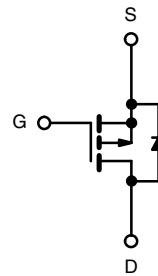
- TrenchFET[®] Power MOSFET



RoHS
COMPLIANT



Ordering Information: Si7489DP-T1-E3 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 100	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 28 ^a	
		T _C = 70 °C	- 24.9 ^a	
		T _A = 25 °C	- 7.8 ^{b, c}	
		T _A = 70 °C	- 6.2 ^{b, c}	
Pulsed Drain Current	I _{DM}	- 40	A	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		- 28 ^a
		T _A = 25 °C		- 4.3 ^{b, c}
Avalanche Current	I _{AS}	- 35		mJ
Single-Pulse Avalanche Energy	E _{AS}	61		
Maximum Power Dissipation	P _D	T _C = 25 °C	83	
		T _C = 70 °C	53	
		T _A = 25 °C	5.2 ^{b, c}	
		T _A = 70 °C	3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	19	24	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	1.2	1.5	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 sec.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 65 °C/W.

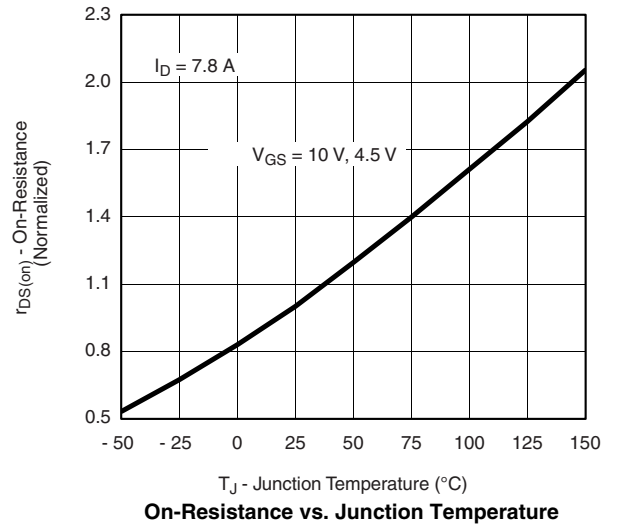
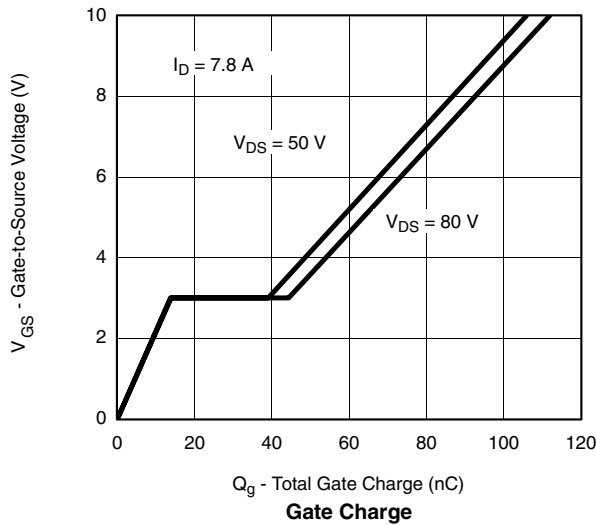
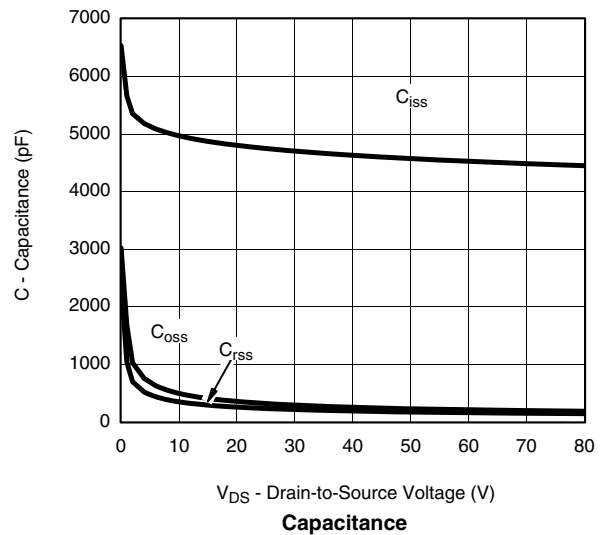
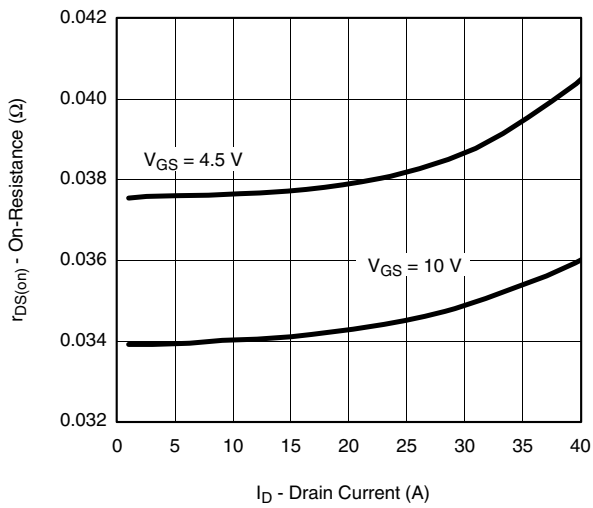
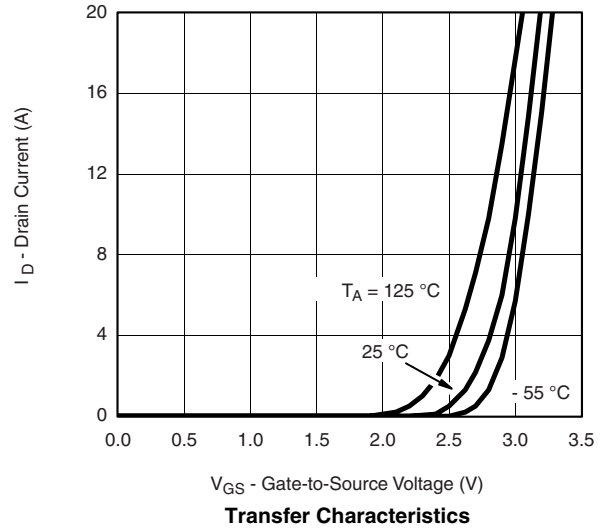
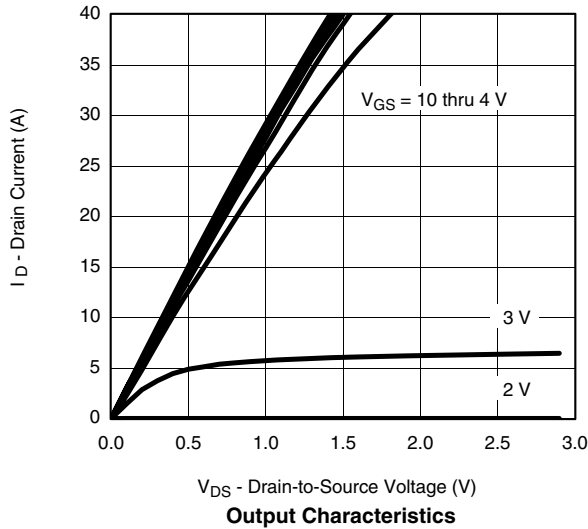
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 113		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		5.5			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	- 40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -7.8\text{ A}$		0.033	0.041	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -7.3\text{ A}$		0.038	0.047	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -7.8\text{ A}$		38		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4600		pF
Output Capacitance	C_{oss}		230			
Reverse Transfer Capacitance	C_{riss}		175			
Total Gate Charge	Q_g	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -7.8\text{ A}$		106	160	nC
				54	81	
Gate-Source Charge	Q_{gs}	$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -7.8\text{ A}$		14		nC
Gate-Drain Charge	Q_{gd}		26			
Gate Resistance	R_g		$f = 1\text{ MHz}$		4	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 8.1\text{ }\Omega$ $I_D \cong -6.2\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r		20	30		
Turn-Off Delay Time	$t_{d(off)}$		110	165		
Fall Time	t_f		100	150		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 8.1\text{ }\Omega$ $I_D \cong -6.2\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		42	65	
Rise Time	t_r		160	240		
Turn-Off Delay Time	$t_{d(off)}$		100	150		
Fall Time	t_f		100	150		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			- 28	A
Pulse Diode Forward Current ^a	I_{SM}				- 40	
Body Diode Voltage	V_{SD}	$I_S = -6.2\text{ A}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -6.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		60	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}		150	225	nC	
Reverse Recovery Fall Time	t_a		46		ns	
Reverse Recovery Rise Time	t_b		14			

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

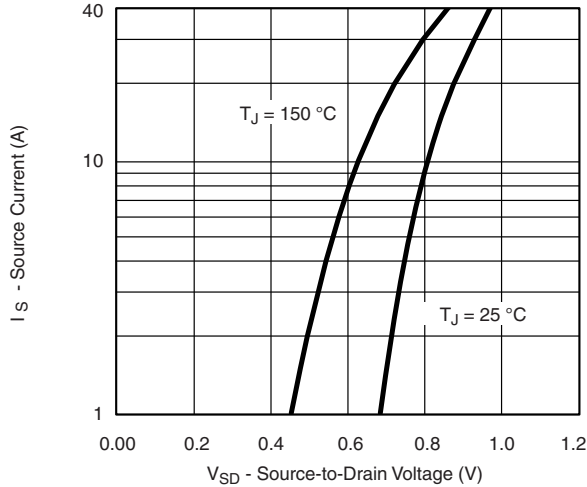
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

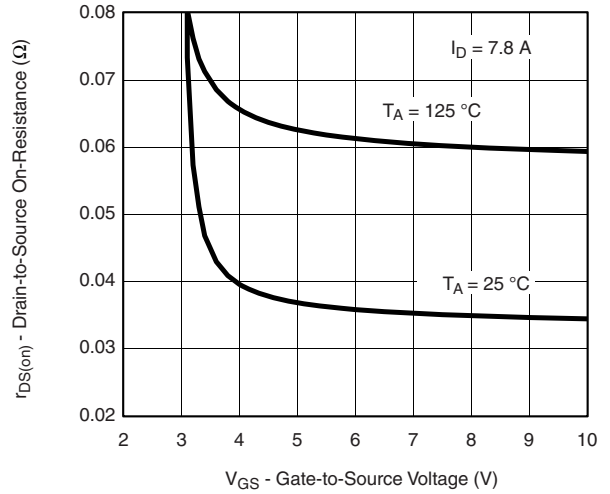




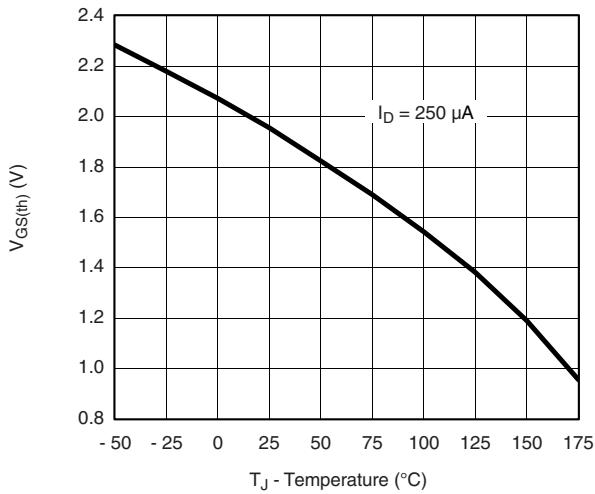
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



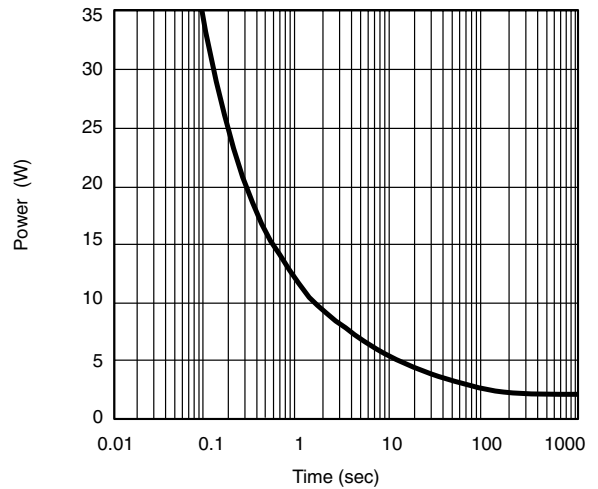
Source-Drain Diode Forward Voltage



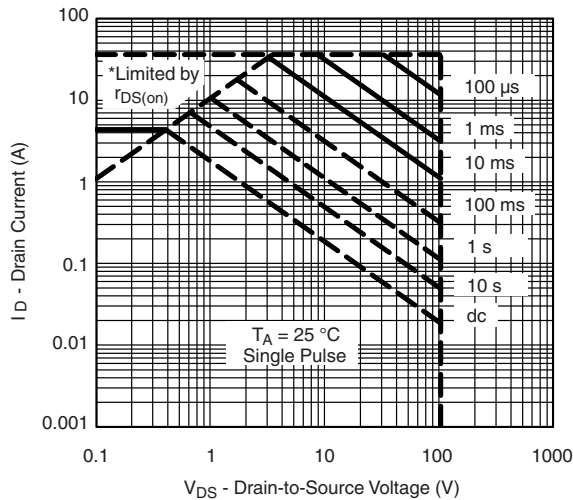
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

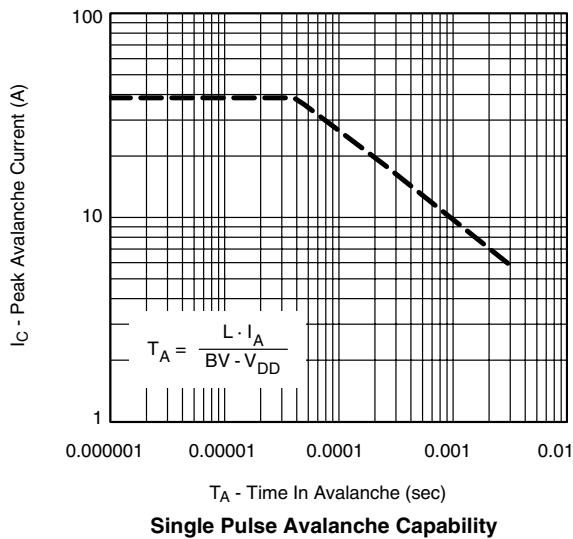
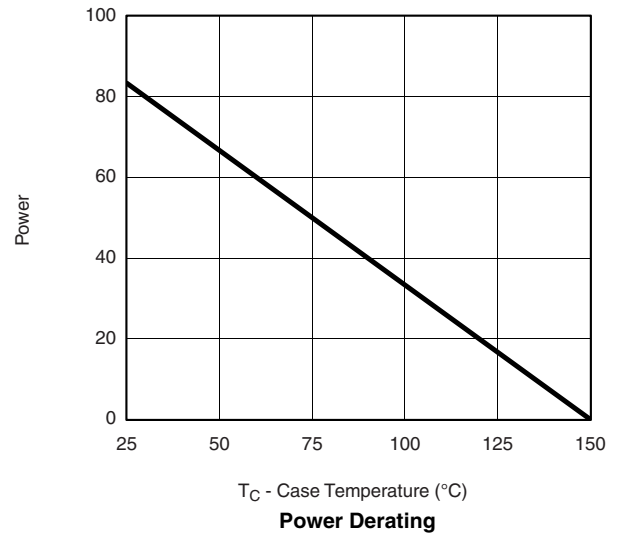
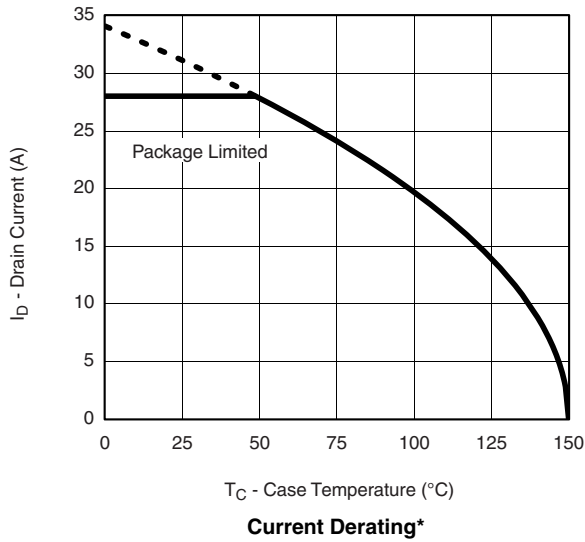


* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



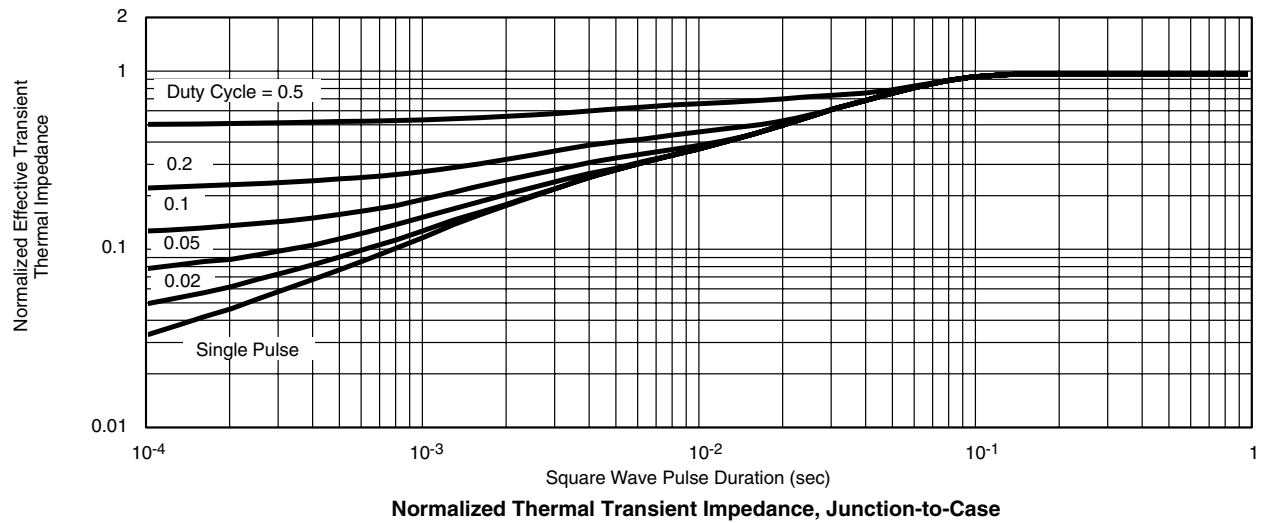
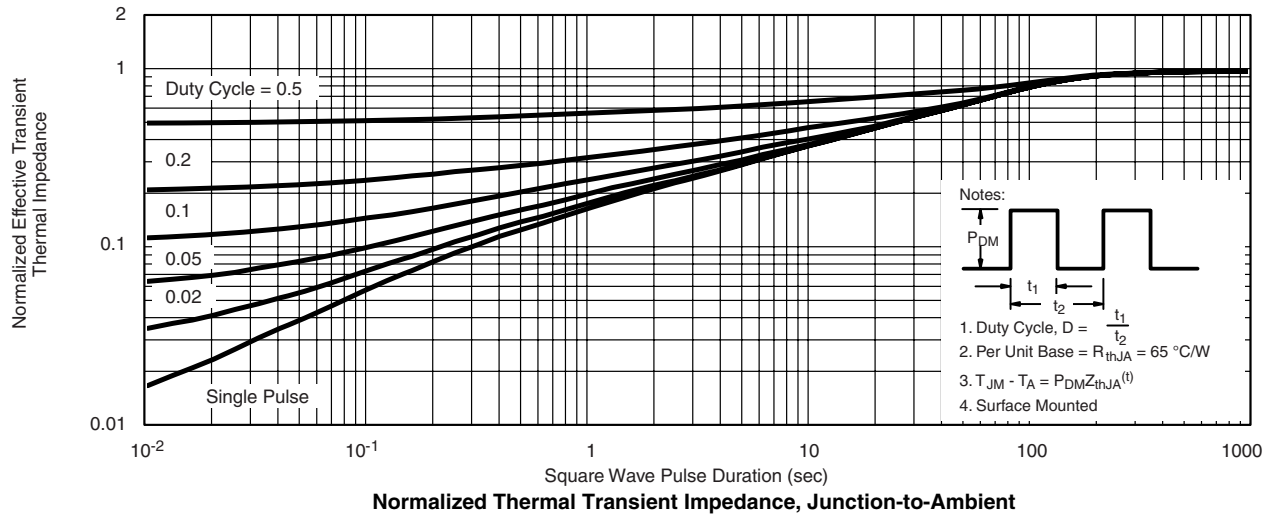
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



*The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73436>.



Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.