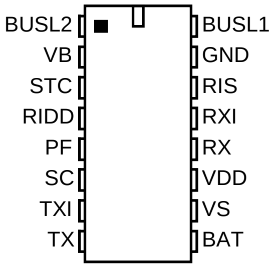
- **Meter-Bus Transceiver (for Slave) meets standard EN1434-3**
- **Receiver logic with dynamic level recognition**
- **Adjustable constant current sink via resistor**
- **Polarity independent**
- **Power fail function**
- **Module supply voltage switch**
- **3.3 V constant voltage source**
- **Remote powering**
- **Up to 9600 baud in half duplex for UART protocol**
- **Slave Power Support**
  - **supply from Meter-Bus via output VDD**
  - **supply from Meter-Bus via output VDD or from back up battery**
  - **supply from battery – Meter-Bus active for data transmission only**

D PACKAGE
(TOP VIEW)



description

TSS721A is a single chip transceiver developed for Meter-Bus standard (EN1434-3) applications.

The TSS721A interface circuit adjusts the different potentials between a slave system and the Meter-Bus master. The connection to the Bus is polarity independent and supports full galvanic slave isolation with opto-couplers.

The circuit is supplied by the master via the bus. Therefore this circuit offers no additional load for the slave battery. A power-fail function is integrated.

The receiver has dynamic level recognition, and the transmitter a programmable current sink.

A 3.3-V voltage regulator, with power reserve for a delayed switch off at bus fault, is integrated.

function (the functional description refers to typical values)

Data Transmission Master to Slave

The mark level on the bus lines V_{BUS} = MARK is defined by the difference of BUSL1 and BUSL2 at the slave. It is dependent on the distance of Master to Slave, which affects the voltage drop on the wire. To make the receiver independent, a dynamic reference level on the SC pin is used for the voltage comparator TC3 (refer to figure 1).

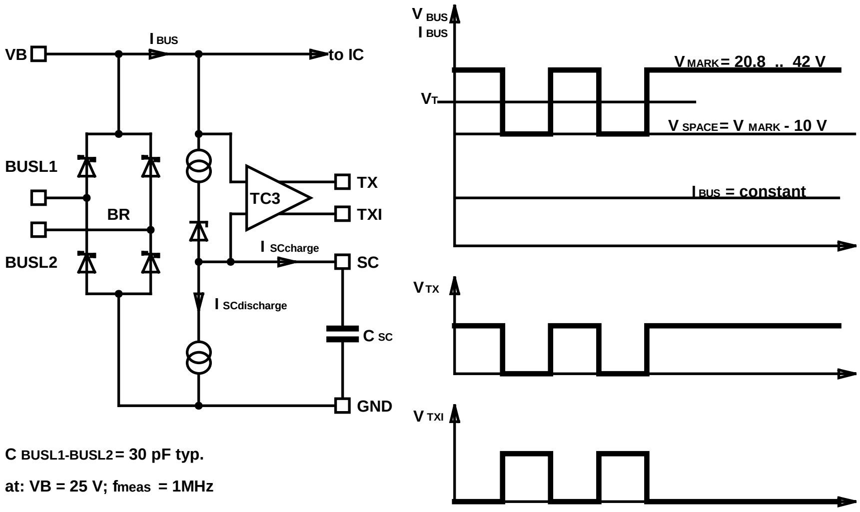


Figure 1

A capacitor C_{SC} at pin SC is charged by a current $I_{SCcharge}$ and is discharged with a current $I_{SCdischarge}$ where:

$$I_{SCdischarge} = \frac{I_{SCcharge}}{40\,(typ.)}$$

This ratio is necessary to run any kind of UART protocol independent of the data contents. (e. g. if an 11-Bit UART protocol is transmitted with all data bits at '0' and only the stop bit at '1'). There must be sufficient time to recharge the capacitor C_{SC}. The input level detector TC3 detects voltage modulations from the master, V_{BUS} = SPACE/MARK conditions and switches the inverted output TXI and the non-inverted output TX.

Data Transmission Slave to Master

The device uses current modulation to transmit information from Slave to the Master while the bus voltage remains constant. The current source CS3 modulates the bus current and the master detects the modulation. The constant current source CS3 is controlled by the inverted input RXI or the non-inverted input RX. The current source CS3 can be programmed by an external resistor R_{RIS}. The modulation supply current I_{MS} flows in addition to the current source CS3 during the modulation time.

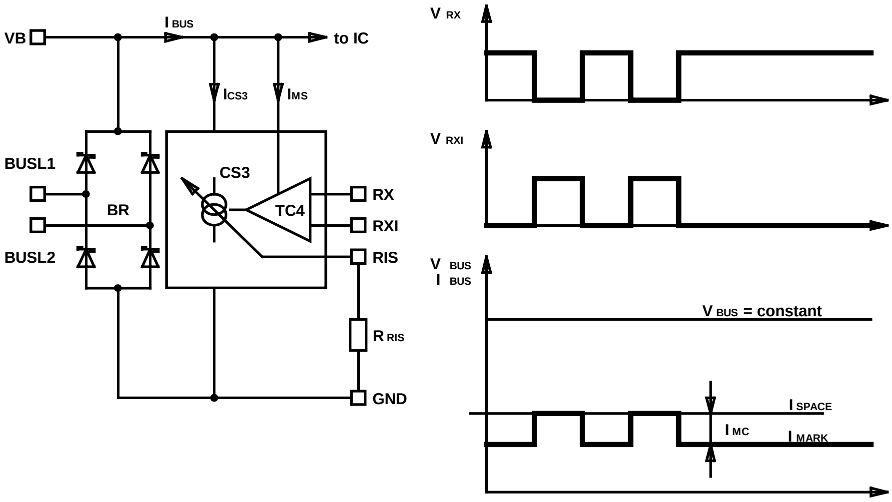


Figure 2

$$I_{MC} = I_{MS} + I_{CS3}$$

Since the TSS721A is configured for half-duplex only, the current modulation from RX or RXI is repeated concurrently as ECHO on the outputs TX and TXI. If the Slave, as well as the Master, is trying to send information via the lines, the added signals appear on the outputs TX and TXI which indicate the data collision to the slave (refer to figure 6).

The bus topology requires a constant current consumption by each connected slave.

To calculate the value of the programming resistor R_{RIS}, use the following formula:

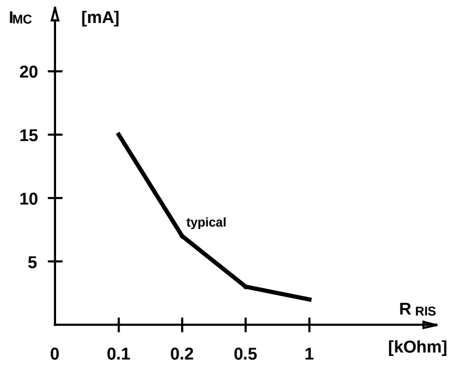


Figure 3

$$R_{RIS} = \frac{V_{RIS}}{I_{CS3}} = \frac{V_{RIS}}{I_{MC} - I_{MS}}$$

V_{RIS} - voltage on pin RIS
R_{RIS} - programming resistor
I_{CS3} - programmable current
I_{MC} - modulation current
I_{MS} - modulation supply current (typical 220 µA)

Slave Supply 3.3-V

The TSS721A has the 3.3-V voltage regulator. The output power of this voltage regulator is supplied by the storage capacitor C_{STC} at pin STC. The storage capacitor C_{STC} at Pin STC is charged with constant current I_{STC_use} from the current source CS1. The maximum capacitor voltage is limited to REF1. The charge current I_{STC} has to be defined by an external resistor at Pin R_{IDD}.

The adjustment resistor R_{RIDD} can be calculated using the following formula:

$$R_{RIDD} = 25\ \frac{V_{RIDD}}{I_{STC}} = 25\ \frac{V_{RIDD}}{I_{STC\_use} + I_{CI1}}$$

I_{STC} - current from current source CS1
I_{STC_use} - charge current for support capacitor
I_{CI} - internal current
V_{RIDD} - voltage on pin R_{IDD}
R_{RIDD} - value of adjustment resistor

The voltage level of the storage capacitor C_{STC} is monitored with comparator TC1. Once the voltage V_{STC} reaches V_{VDD_on}, the switch S_{VDD} connects the stabilised voltage V_{VDD} to pin V_{DD}. V_{DD} is turned off if the voltage V_{STC} drops below the V_{VDD_off} level.

Voltage variations on the capacitor C_{STC} create bus current changes:

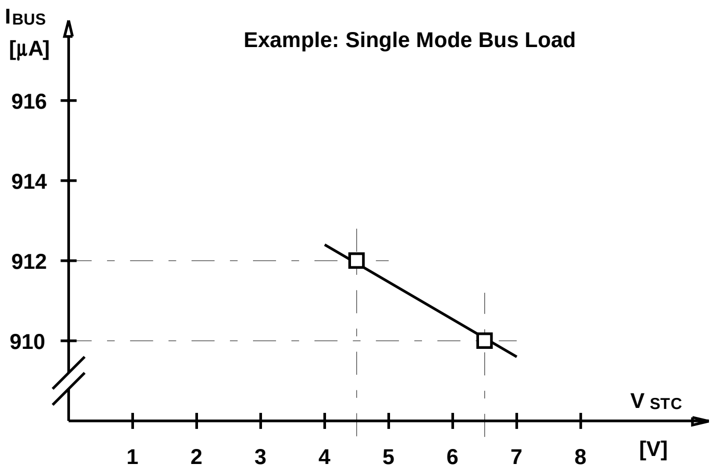


Figure 4

At a bus fault the shut down time of V_{DD} (t_{off}) in which data storage can be performed depends on the system current I_{VDD} and the value of capacitor C_{STC}. Refer to Figure 5, which shows a correlation between the shut down of the bus voltage V_{BUS} and V_{DD_off} and t_{off} for dimensioning the capacitor.

The output VS is meant for slave systems which are driven by the bus energy, as well as from a battery should the busline voltage fail. The switching of VS is synchronised with V_{DD} and is controlled by the comparator TC1. An external transistor at the output VS allows switching from the Meter-Bus remote supply to battery.

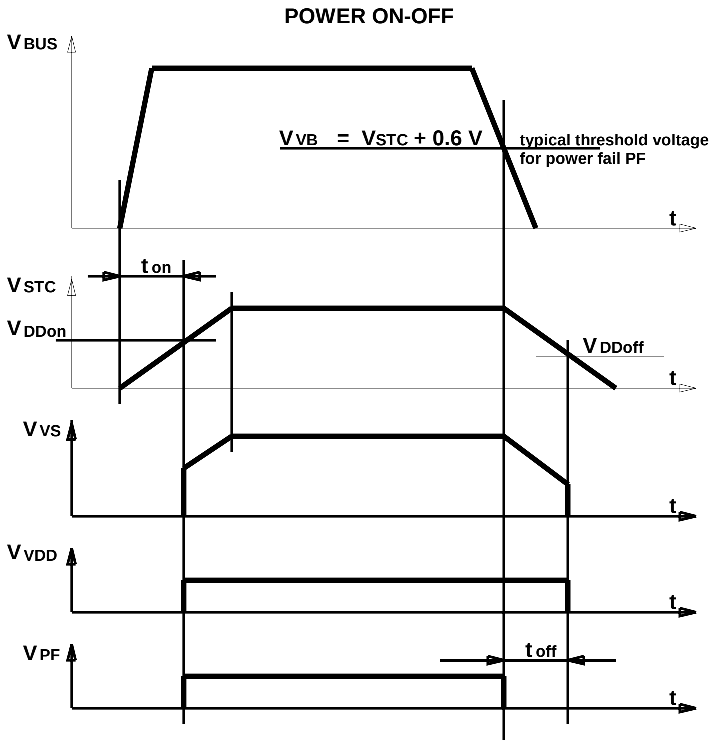


Figure 5

$$t_{off} = C_{STC}\frac{V_{STC} - V_{VDDoff}}{I_{VDD} + I_{CI1}}$$

Power Fail Function

Owing to the rectifier bridge BR at the input, BUSL1 and BUSL2, the TSS721A is polarity independent. The pin VB to ground (GND) delivers the bus voltage V_{VB} less the voltage drop over the rectifier BR. The voltage comparator TC2 monitors the bus voltage. If the voltage V_{VB} > V_{STC} + 0.6 V, then the output PF = '1'. The output level PF = '0' (power fail) provides a warning of a critical voltage drop to the microcontroller to save the data immediately.

functional schematic

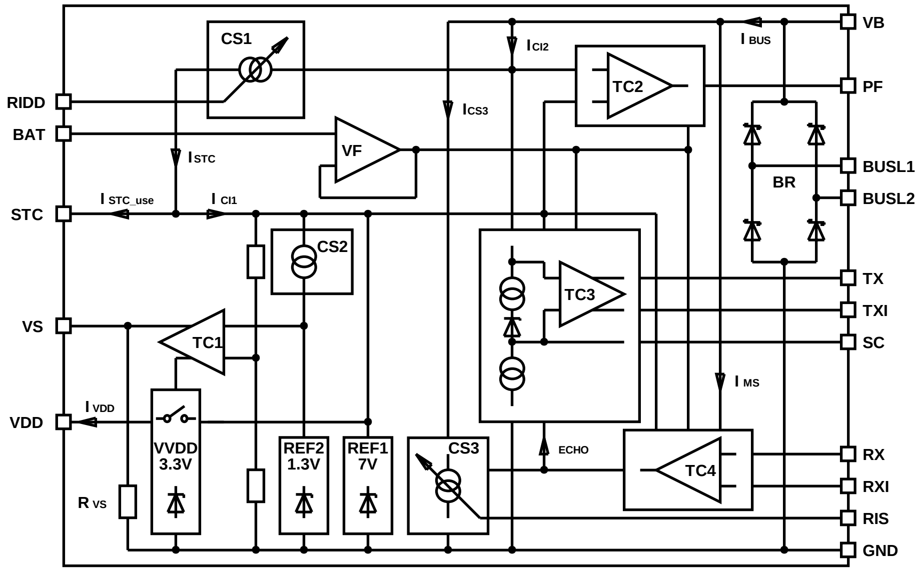


Figure 6

pinning	pin	function
1	BUSL2	Meter-Bus
2	VB	differential bus voltage after rectifier
3	STC	support capacitor
4	RIDD	current adjustment input
5	PF	power fail output
6	SC	sampling capacitor
7	TXI	data output inverted
8	TX	data output
9	BAT	logic level adjust
10	VS	switch for bus or battery supply output
11	VDD	voltage regulator output
12	RX	data input
13	RXI	data input inverted
14	RIS	adjust input for modulation current
15	GND	ground
16	BUSL1	Meter-Bus

absolute maximum ratings

Voltage BUSL1 to BUSL2	|50| V
Input voltage at RX and RXI	- 0.3 to 5.5 V
Input voltage at pin UBAT	- 0.3 to 5.5 V
Operating junction temperature	- 25 to 150 °C
Operating temperature free-air	- 25 to 85 °C
Storage temperature	- 65 to 150 °C
Power derating factor junction to ambient	8.0 mW/°C

recommended operating conditions

Parameter		min	max	unit
Bus voltage |BUSL2-BUSL1|	Receiver	10.8	42.0	V
	Transmitter	12.0	42.0	V
V_B voltage (receive mode)		9.3		V
R_{IDD} Resistor		13	80	kΩ
R_{IS} Resistor		100		Ω
V_{BAT}, (see Note 1)		2.5	3.8	V
Operating free-air temperature		-25	85	° C

NOTE: All voltage values are measured with respect to the GND terminal unless otherwise noted.
NOTE 1: $V_{BATmax} <= V_{STC} - 1V$

electrical characteristics at recommended ranges (unless otherwise noted)

Parameter	Test conditions	min	typ	max	unit
V drop Rectifier BR	I_{BUS}=3mA			1.5	V
V drop current source CS1	R_{IDD}=13 kΩ			1.8	V
I_{BUS}	V_{STC}=6.5 V; I_{MC}=0 mA R_{IDD}=13 kΩ			3.0	mA
	V_{STC}=6.5 V; I_{MC}=0 mA R_{IDD}=30 kΩ			1.5	mA
ΔI_{BUS}	ΔV_{BUS}=10 V; I_{MC}=0 mA R_{IDD}=13 – 30 kΩ			2	%
I_{CC}	V_{STC}=6.5 V; I_{MC}=0 mA; V_{BAT}=3.8 V; R_{IDD}=13 kΩ; (see Note 2)			650	µA
I_{CI1}	V_{STC}=6.5 V; I_{MC}=0 mA; V_{BAT}=3.8 V; R_{IDD}=13 kΩ; V_{BUS}=6.5 V; RX/RXI=off (See Note 2)			350	µA
I_{BAT}		-0.5		0.5	µA
I_{BAT} + I_{VDD}	V_{BUS}=0 V; V_{STC}=0 V	- 0.5		0.5	µA
V_{VDD}	-I_{VDD}=1 mA; V_{STC}=6.5 V	3.1		3.4	V
R_{VDD}	-I_{VDD}=2 to 8 mA; V_{STC}=4.5V			5.0	Ω
V_{STC}	V_{DD}=on and VS=on	5.6		6.4	V
	V_{DD}=off and VS=off	3.8		4.3	V
V_{STC}	(See Note 3)	6.5		7.5	V
I_{STC_use}	R_{IDD}=30 kΩ; V_{STC}=5 V	0.65		1.1	mA
	R_{IDD}=13kΩ; V_{STC}=5 V	1.85		2.4	mA
V_{RIDD}	R_{IDD}=30 kΩ;	1.23		1.33	V
V_{VS}	V_{DD}=on; I_{VS}=-5 µA	V_{STC} -0.4		V_{STC}	V
R_{VS}	V_{DD}=off	0.3		1.0	MΩ
V_{PF}	V_{STC}= 6.5V; V_{VB}=V_{STC}+0.8 V; I_{PF}= -100 µA	V_{BAT}- 0.6		V_{BAT}	V
	V_{STC}= 6.5V; V_{VB}=V_{STC}+0.3 V; I_{PF}=1 µA	0		0.6	V
	V_{STC}= 6.5V; V_{VB}=V_{STC}+0.3 V; I_{PF}=5 µA	0		0.9	V
t_{on}	C_{STC} = 50 µF, (see Note 4)			3	s

NOTE: All voltage values are measured with respect to the GND terminal unless otherwise noted.
NOTES: 2. Inputs RX/RXI and outputs TX/TXI are open; I_{CC} = I_{CI1} + I_{CI2}
3. I_{VDD} < I_{STC_use}
4. Bus voltage slew rate: 1V/µs

electrical characteristics at recommended ranges (unless otherwise noted)

RECEIVER SECTION

Parameter	test conditions	min	typ	max	unit
V_T		MARK - 8.2		MARK - 5.7	V
V_{SC}				V_{VB}	V
$I_{SCcharge}$	V_{SC}=24 V; V_{VB}=36 V	-15		-40	µA
$I_{SCdischarge}$	V_{SC}=V_{VB}=24 V	0.3		-0.033 x $I_{SCcharge}$	µA
V_{OH} (TX; TXI)	I_{TX}/I_{TXI}=-100 µA See fig. 1	V_{BAT} - 0.6		V_{BAT}	V
V_{OL} (TX; TXI)	I_{TX}/I_{TXI}=100 µA	0		0.5	V
	I_{TX}=1.1 mA	0		1.5	V
I_{TX}; I_{TXI}	V_{TX}=7.5; V_{VB}=12V; V_{STC}=6.0V; V_{BAT}=3.8V			10	µA

TRANSMITTER SECTION

Parameter	Test conditions	min	typ	max	unit
I_{MC}	R_{RIS}=100 Ω	11.5		19.5	mA
V_{RIS}	R_{RIS}=100 Ω	1.4		1.7	V
	R_{RIS}=1000 Ω	1.5		1.8	V
V_{IH} (RX; RXI)	See fig. 2 See Note 5	V_{BAT}-0.8		5.5	V
V_{IL} (RX; RXI)	See fig. 2	0		0.8	V
I_{RX}	V_{RX}=V_{BAT}=3 V; V_{VB}=V_{STC}=0 V	-0.5		0.5	µA
	V_{RX}=0 V; V_{BAT}=3 V; V_{STC}=6.5 V	-10		-40	µA
I_{RXI}	V_{RXI}=V_{BAT}=3 V; V_{VB}=V_{STC}=0 V	10		40	µA
	V_{RXI}=V_{BAT}=3 V; V_{STC}=6.5 V	10		40	µA

NOTE: All voltage values are measured with respect to the GND terminal unless otherwise noted.
NOTE 5: V_{IHmax} = 5.5 V is valid only for the following condition: V_{STC}>=6.5 V.

APPLICATIONS

basic application circuit for using of support capacitor C_{STC} > 50 µF

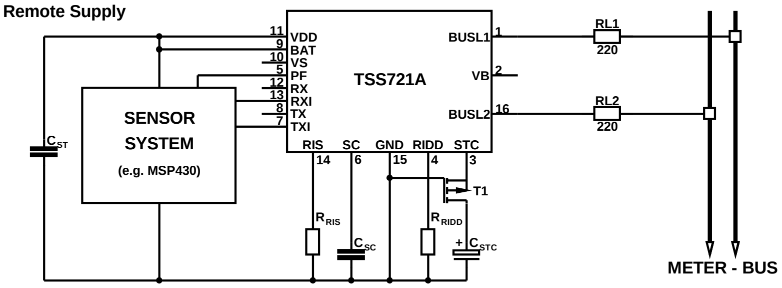


Figure 7

R_{RIDD} = 30 kΩ	C_{STC} =< 220 µF	single load 1UL
R_{RIDD} = 13 kΩ	C_{STC} =< 470 µF	double load 2UL

NOTE: Used Transistor T1 e.g. BSS84.

basic application circuit for supply from battery

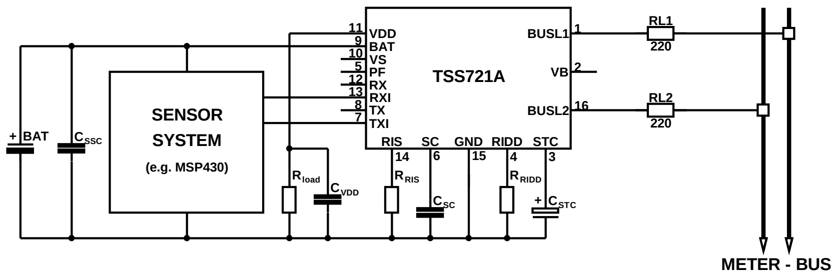


Figure 8

C_{SSC} - system stabilising capacitor
C_{STC} - support capacitor
C_{SC} - sampling capacitor
C_{VDD} - stabilising capacitor (100 nF)
C_{STC} : C_{VDD} > = 4:1

R_{RIDD} - slave-current adjustment resistor
R_{RIS} - modulation-current resistor
RL1, RL2 - protection resistors
R_{load} - discharge resistor (100 kΩ recommended)

basic applications for different supply modes

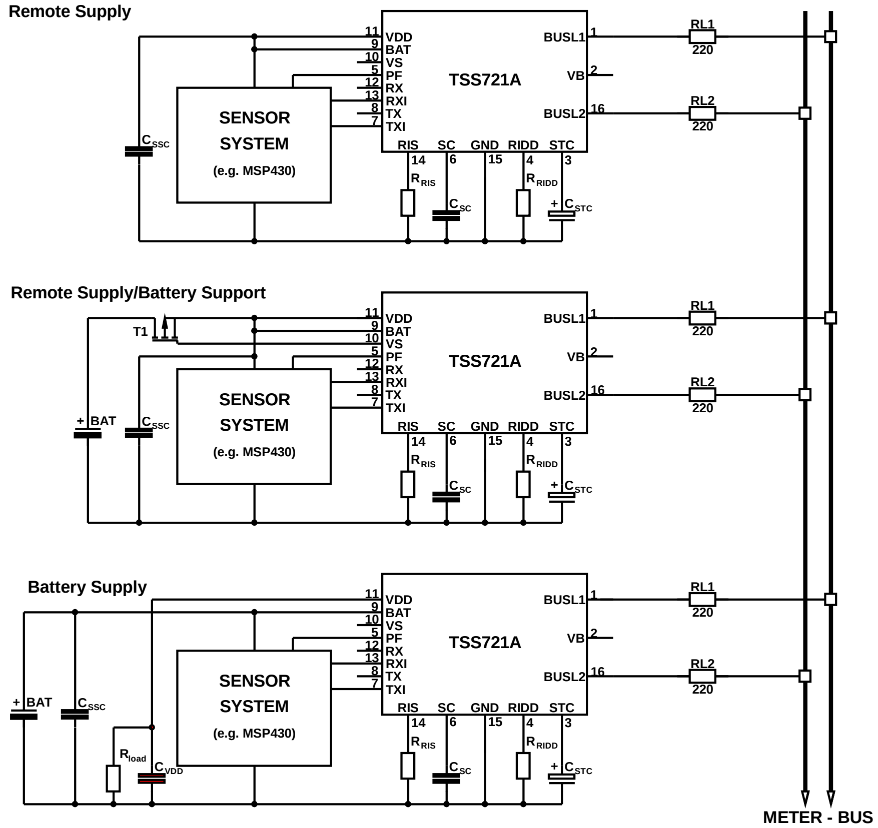


Figure 9

NOTE: Please watch R_{DSon} of the transistor T1 (e.g. BSS84) at low level battery voltage.

basic optocoupler application

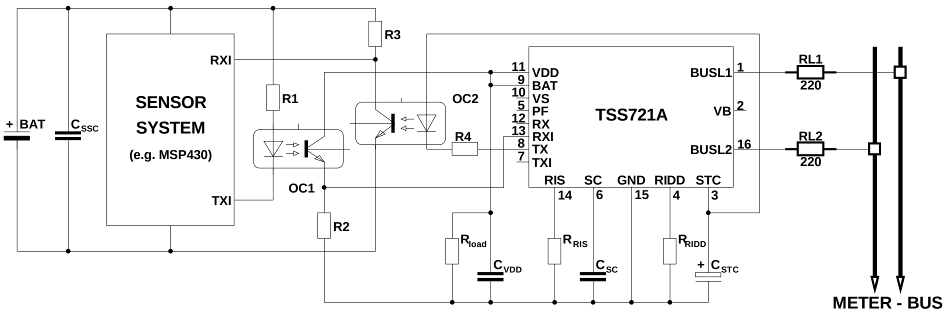
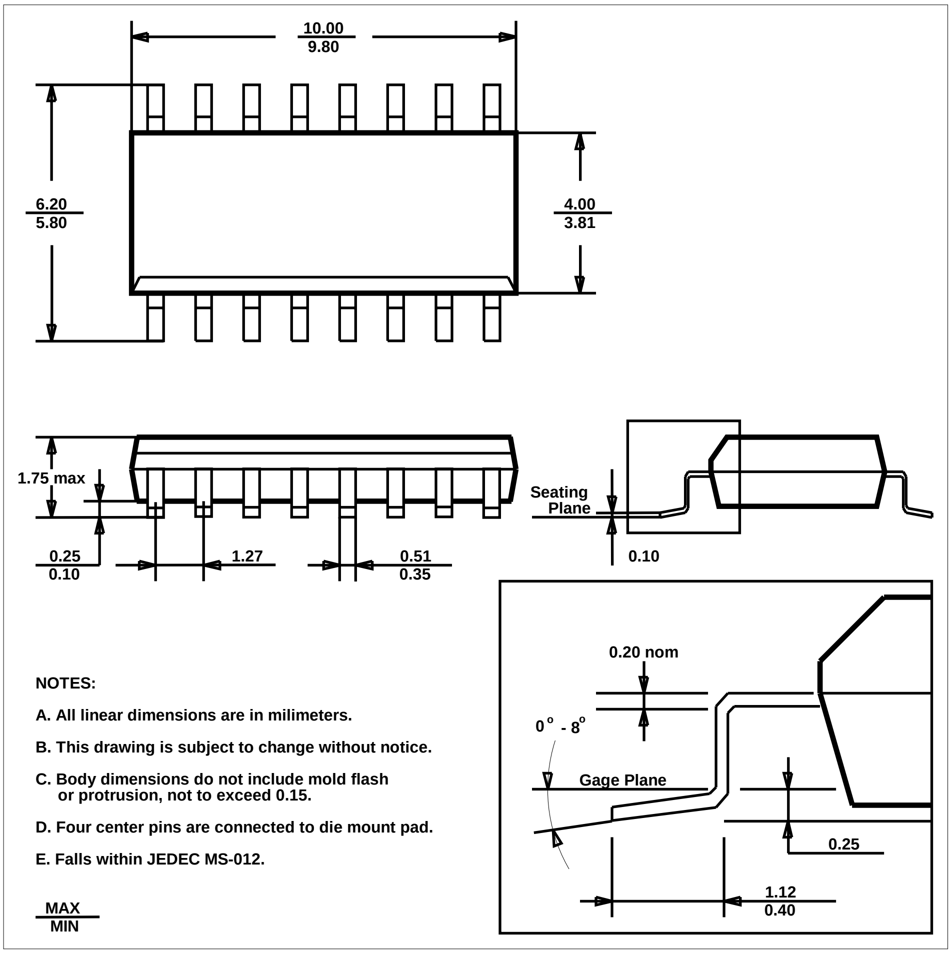


Figure 10

MECHANICAL DATA

D(R-PDSO-G)** **PLASTIC SMALL OUTLINE PACKAGE**



NOTES:

A. All linear dimensions are in milimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

D. Four center pins are connected to die mount pad.

E. Falls within JEDEC MS-012.

Figure 11