SP9210

200MHz DUAL 4-BIT LATCH

The SP9210 is a dual 4-bit master/slave D-type flip-flop with asynchronous set and reset which override the clock input.

Data is entered into the master when the clock is low and is transferred to the slave on the positive transition of the clock, the device being edge-sensitive.

On-chip pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- Dual 4-Bit Master/Slave D-Type Flip-Flop
- Clock Rate in Excess of 200MHz
- -5.2V Supply
- Current Consumption Typically 145mA
- Input Current Less Than 330µA
- Operating Temperature Range -30°C to +85°C
- Set and Reset Inputs Provided
- ECL 10K Compatible
- Dual Clock Inputs

ORDERING INFORMATION

SP9210DG (Industrial - Ceramic DIL package)
SP9210BB DG (Plessey High Reliability Ceramic DIL package)

PIN NAMES

S1-4	Set input for 1-4
S5-8	Set input for 5-8
V_{EE}	Supply voltage (-VE)
D1-8	Data inputs 1-8
CLK1-4	Clock latch for 1-4
CLK5-8	Clock latch for 5-8
Q1-8	Outputs latches 1-8
R1-4	Reset input latch for 1-4
R5-8	Reset input latch for 5-8

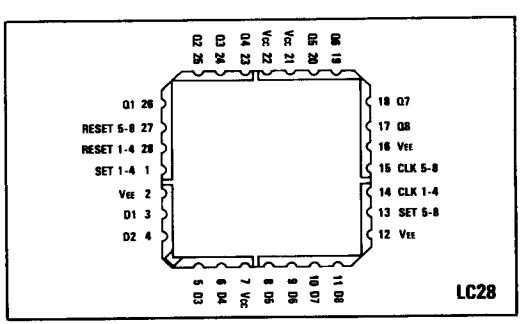


Fig.1(b) Pin connections, surface mounting package (top view)

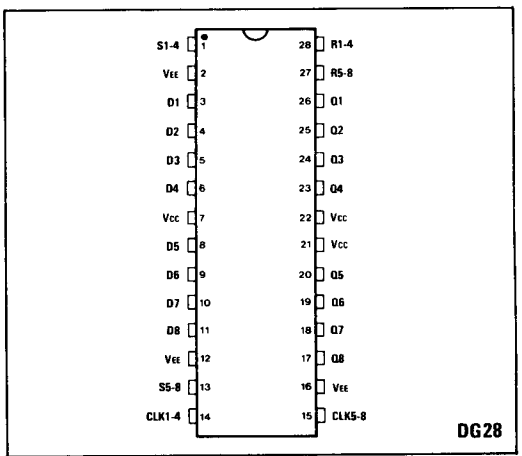


Fig.1(a) Pin connections, ceramic DIL package (top view)

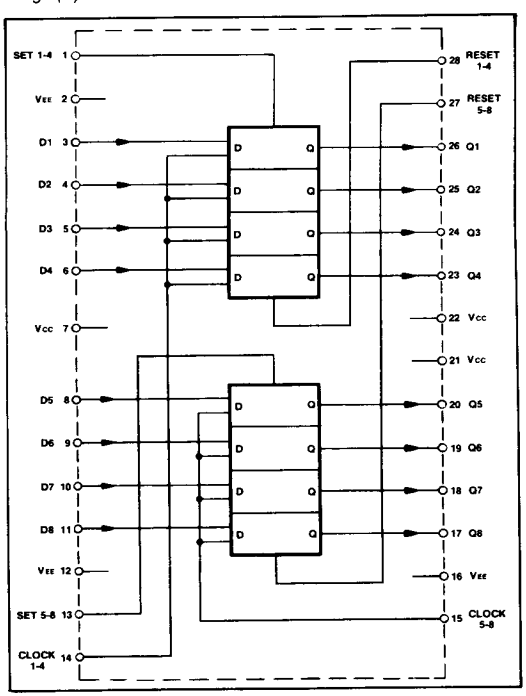


Fig.2 SP9210 block diagram

ELECTRICAL CHARACTERISTICS

Each circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

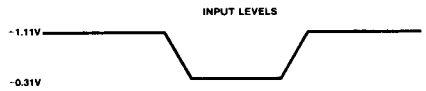
Test temp.	TEST VOLTAGES (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
-30°C	-0.89	-1.89	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.70	-1.825	-1.035	-1.440	-5.2

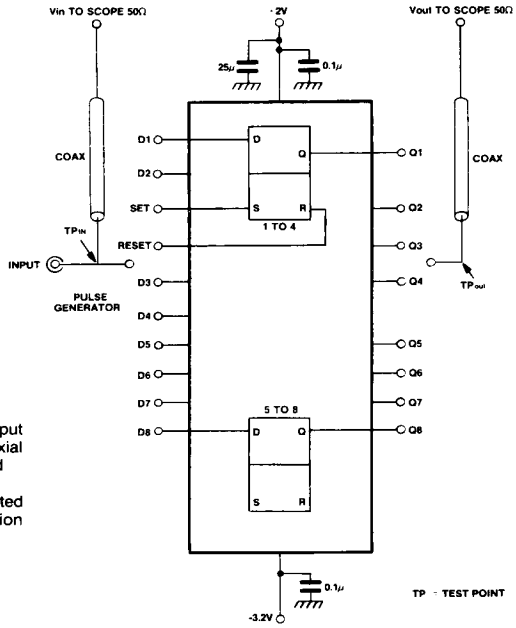
Characteristic	Symbol	Pin under test	-30°C Min.	-30°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX.	V_{IL} MIN.	V_{IHA} MIN.	V_{ILA} MAX.	V_{EE}	V_{CC} (GND)
POWER SUPPLY																
Drain current	I_{EE}	2,12,16	-	200	-	145	180	-	200	mA	-	-	-	-	2,12,16	7,21,22
Input current	I_{INH}	Set/Reset	-	-	-	-	330	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
		Clock	-	-	-	-	310	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
		Data	-	-	-	-	310	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
Input leakage current	I_{INL}	All inputs	-	-	0.5	-	-	-	-	µA	-	Note 1	-	-	2,12,16	7,21,22
Logic '1' output voltage	V_{OH}	All outputs (Note 2)	-1.06	-0.89	-0.96	-	-0.81	-0.89	-0.70	V	Data inputs	-	-	-	2,12,16	7,21,22
Logic '0' output voltage	V_{OL}	All outputs (Note 2)	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	-	Data inputs	-	-	2,12,16	7,21,22
Logic '1' threshold voltage	V_{OHA}	All outputs (Note 2)	-1.08	-	-0.98	-	-	-0.91	-	V	-	-	Data inputs	-	2,12,16	7,21,22
Logic '0' threshold voltage	V_{OLA}	All outputs (Note 2)	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	-	Data inputs		
SWITCHING TIMES											**+1.11V**	**+0.3V**	**Pulse in**	**Pulse out**	**-3.2V**	**+2.0V**
Clock input propagation delay	t_{d+}	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22
	t_{d-}	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	-	Data inputs	Clock inputs	Outputs	2,12,16	7,21,22
Rise time (20 % - 80 %)	t_r	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22
Fall time (20 % - 80 %)	t_f	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	-	Data inputs	Clock inputs	Outputs	2,12,16	7,21,22
Set propagation delay	t_{set}	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	-	Set inputs	Outputs	2,12,16	7,21,22
Reset propagation delay	t_{rset}	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	-	Reset inputs	Outputs	2,12,16	7,21,22
Set up time	t_s	Data inputs	1.5	-	1.5	-	-	1.5	-	ns	-	-	Data,Clock	Outputs	2,12,16	7,21,22
Hold time	t_h	Data inputs	1.0	-	1.0	-	-	1.0	-	ns	-	-	Data,Clock	Outputs	2,12,16	7,21,22
Max.clock frequency	f_{CLK}	All outputs	-	-	200	-	-	-	-	MHz	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22

NOTES
1. Each input pin tested individually.
2. Output level to be measured after a clock pulse has been applied.

Thermal characteristics

DG28	θ_{JA} = 40°C/W
	θ_{JC} = 15°C/W
LC28	θ_{JA} = 70°C/W
	θ_{JC} = 16°C/W

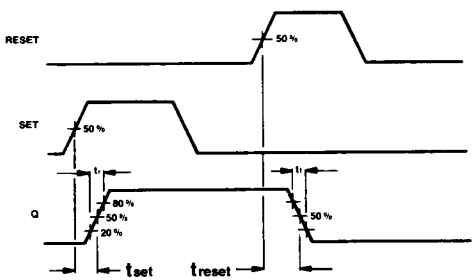




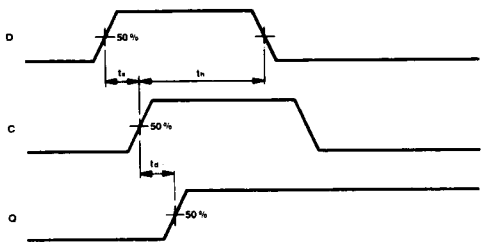
50 ohm to ground located in each scope channel input. All input and output cables to the scope are equal length of 50 ohm coaxial cable. Wire length should be ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

With supply voltages at 2V and -3.2V outputs should be terminated with 50 ohms to ground; this results in an output level translation giving V_{OH} = 1.11V and V_{OL} = +0.31V.

SET AND RESET TIMING DIAGRAM



CLOCK AND DATA TIMING DIAGRAM



NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at data input (D).

Fig.3 Test circuit details for dynamic test

R - S TRUTH TABLE

R	S	Qn + 1
L	L	Qn
L	H	H
H	L	L
H	H	ND

R = Reset, S = Set,
ND = Not defined

CLOCKED TRUTH TABLE

C	D	Qn + 1
L	X	Qn
↓	L	L
↑	H	H

C = Clock, D = Data,
↑ = Rising edge,
X = Don't care

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\|V_{CC} - V_{EE}\|$ 7V
Input voltages	V_{CC} to V_{EE}
Output source current	<40mA
Storage temperature range	-65°C to +150°C
Junction operating temperature	<175°C

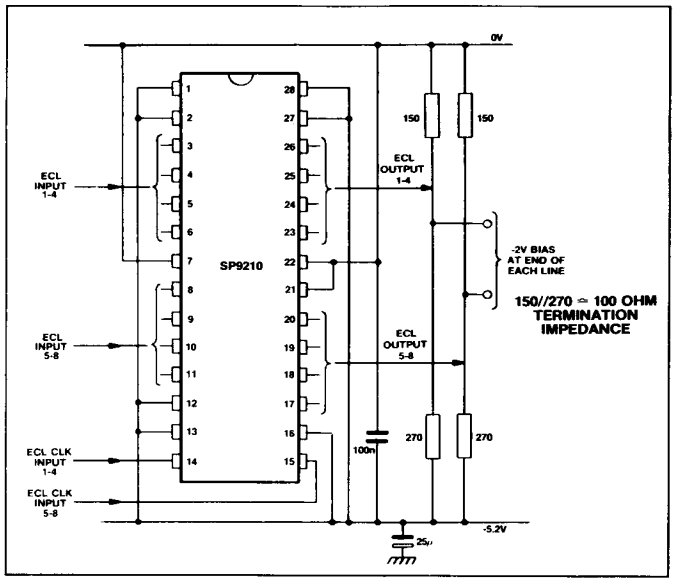


Fig.4 ECL 4 + 4 latch with 100Ω output termination