H85-731

GM76C28A

2,048 WORDS × 8 BIT
CMOS STATIC RAM

Description

The GM76C28A is 2,048 words×8 bits asynchronous, static random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

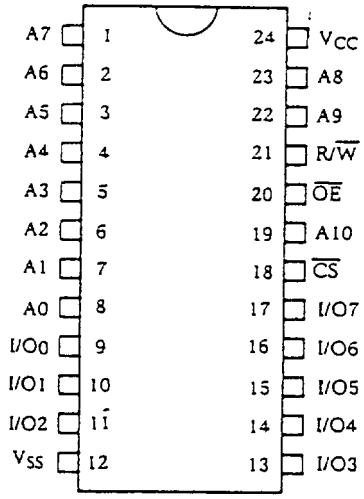
Features

- Access time: 100/120ns
- Low Power Consumption
  Standby: 1μA
  Operation: 25/30mA
- Complete static operation
- Single power supply: 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with Wired-OR capability
- Non-volatile storage with back-up batteries
- Standard 24 DIP, 24 SOP and 24 S-DIP

Pin Description

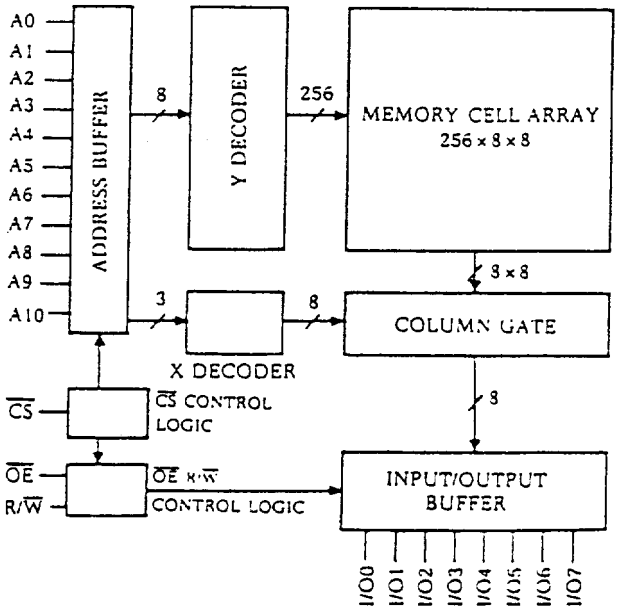
Pin	Function
A0 ~ A10	Address Inputs
R/$\overline{W}$	Read/Write
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O0 ~ 7	Data Input/Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	−65~150	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−0.5~7.0	V
P_D	Power Dissipation	1.0	W

*Note: Operation at or above "Absolute Maximum Ratings" can adversely affect device reliability.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	−0.5	—	0.8	V

*All voltages are referenced to V_{SS} pin=0V.

Truth Table

$\overline{CS}$	$\overline{OE}$	R/$\overline{W}$	A0 to A10	DATA I/O	MODE	I_{CC}
H	X	X	X	Hi-Z	Unselected	I_{CCS1}, I_{CCS2}
L	L	H	Stable	Output Data	Read	I_{CC}
L	H	L	Stable	Input Data	Write	I_{CC}
L	L	L	Stable	Input Data	Write	I_{CC}

Note: X means "H", "L" or "Hi-Z"

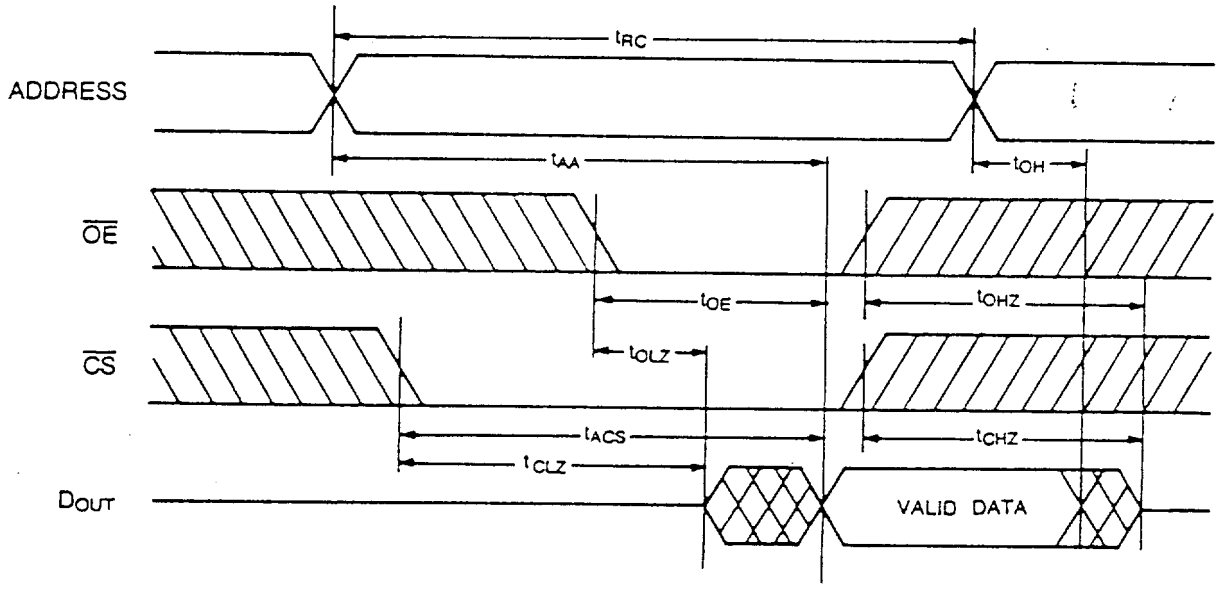
Electrical Characteristics

DC Electrical Characteristics (V_{CC}=5V±10%, V_{SS}=0V, T_A=0~70°C)

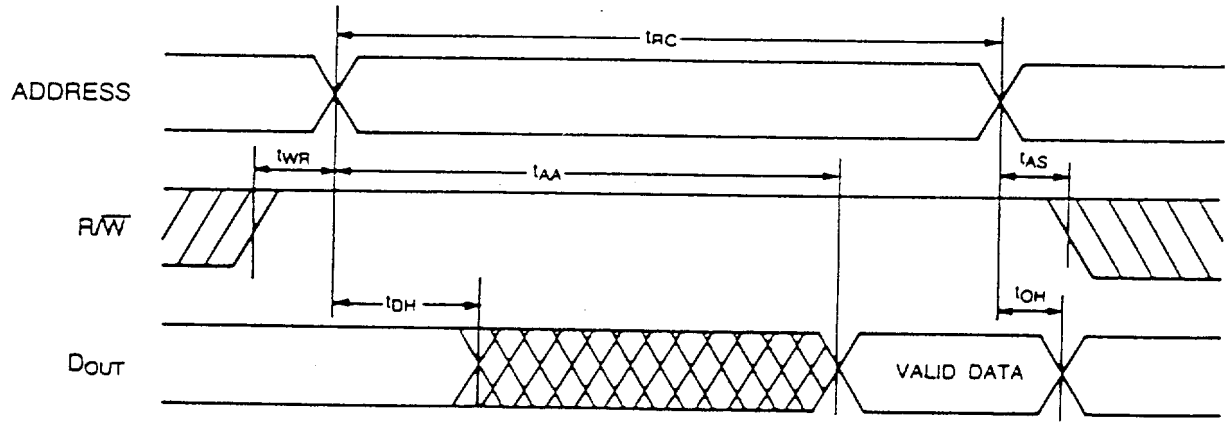
Symbol	Parameter	Conditions	GM76C28A-10			GM76C28A-12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
V_{OL}	Low Level Output Voltage	I_{OL}=4.0mA			0.4			0.4	V
V_{OH}	High Level Output Voltage	I_{OH}=−1.0mA	2.4			2.4			V
I_{CC1}	Operating Supply Current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA		30	60		25	50	mA
I_{CC2}		V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA		16			16		mA
I_{CC}	Average Operating Current	Min cycle, duty=100%, $I_{I/O}$=0mA		30	60		25	50	mA
I_{CCS1}	Standby Supply Current	$\overline{CS}$=V_{IH}		1.5	3.0		1.5	3.0	mA
I_{CCS2}		$\overline{CS}$=V_{CC}-0.2V		1	50		1	50	μA
$I_{I(L)}$	Input Leakage Current	V_{CC}=5.5V, V_I=0 to V_{CC}	−1		1	−1		1	μA
$I_{O(L)}$	Output Leakage Current	$\overline{CS}$=V_{IH}, or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{CC}	−1		1	−1		1	μA

*Typical values are for reference with V_{CC}=5V and T_A=25°C assumed.

READ CYCLE 1 ($\overline{OE}$, $\overline{CS}$ CONTROL, R/$\overline{W}$ = HIGH)



READ CYCLE 2 (R/$\overline{W}$ CONTROL, $\overline{OE}$ = LOW, $\overline{CS}$ = LOW)



AC Electrical Characteristics:

Read Cycle ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

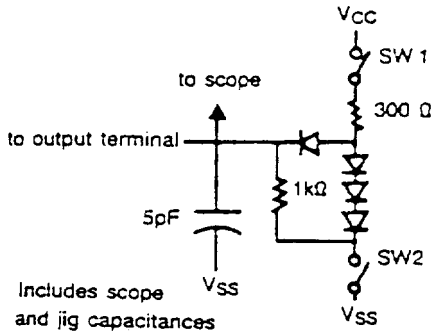
Symbol	Parameter	Conditions	GM76C28A-10		GM76C28A-12		Unit
			Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	100		120		ns
t_{AA}	Address Access Time			100		120	ns
t_{ACS}	$\overline{CS}$ Access Time			100		120	ns
t_{CLZ}	$\overline{CS}$ Output Setup Time	*2	10		10		ns
t_{OE}	$\overline{OE}$ Access Time	*1		55		60	ns
t_{OLZ}	$\overline{OE}$ Output Setup Time	*2	5		10		ns
t_{CHZ}	$\overline{CS}$ Output Floating		0	40	0	40	ns
t_{OHZ}	$\overline{OE}$ Output Floating		0	40	0	40	ns
t_{OH}	Output Hold Time	*1	10		10		ns

Write Cycle: ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

Symbol	Parameter	Conditions	GM76C28A-10		GM76C28A-12		Unit
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	1	100	—	120	—	ns
t_{CW}	Chip Select Time ($\overline{CS}$)		80	—	85	—	ns
t_{AW}	Address Enable Time		80	—	85	—	ns
t_{AS}	Address Setup Time		0	—	0	—	ns
t_{WP}	Write Pulse Width		65	—	70	—	ns
t_{OHZ}	$\overline{OE}$ Output Floating	*2	0	40	0	40	ns
t_{WHZ}	R/W Output Floating	*3	0	45	0	50	ns
t_{DW}	Input Data Setup Time	*1	45	—	50	—	ns
t_{WR}	Address Hold Time		0	—	0	—	ns
t_{DH}	Input Data Hold Time		0	—	0	—	ns
t_{OW}	R/W Output Setup Time	*3	5	—	10	—	ns

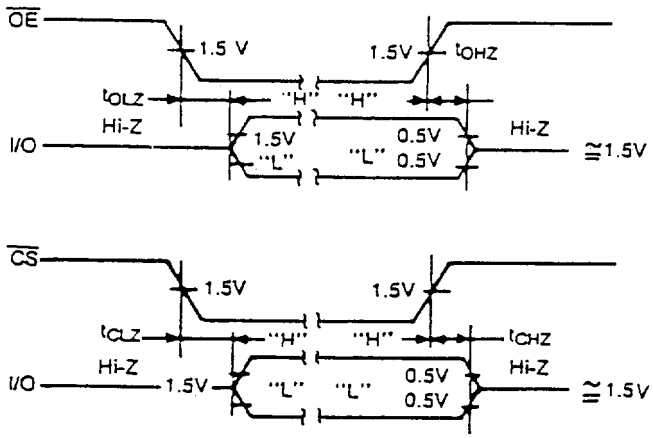
*1 Test conditions.
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Input/output timing reference level: 1.5V
4. Output load: 1 TTL + C_L = 100pF

*2 Test conditions.
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit

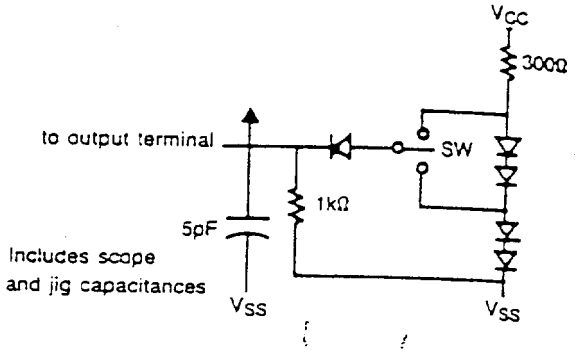


- Both SW1 and SW2 are closed when measuring t_{CHZ} or t_{OHZ}.
- SW1 is open and SW2 is closed when measuring Hi-Z-high of t_{CLZ} or t_{OLZ}
- SW1 is closed and SW2 is open when measuring Hi-Z-low t_{CLZ} or t_{OLZ}

Output turn-on turn-off time

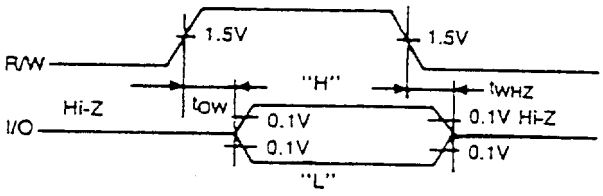


*3 Test conditions.
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit

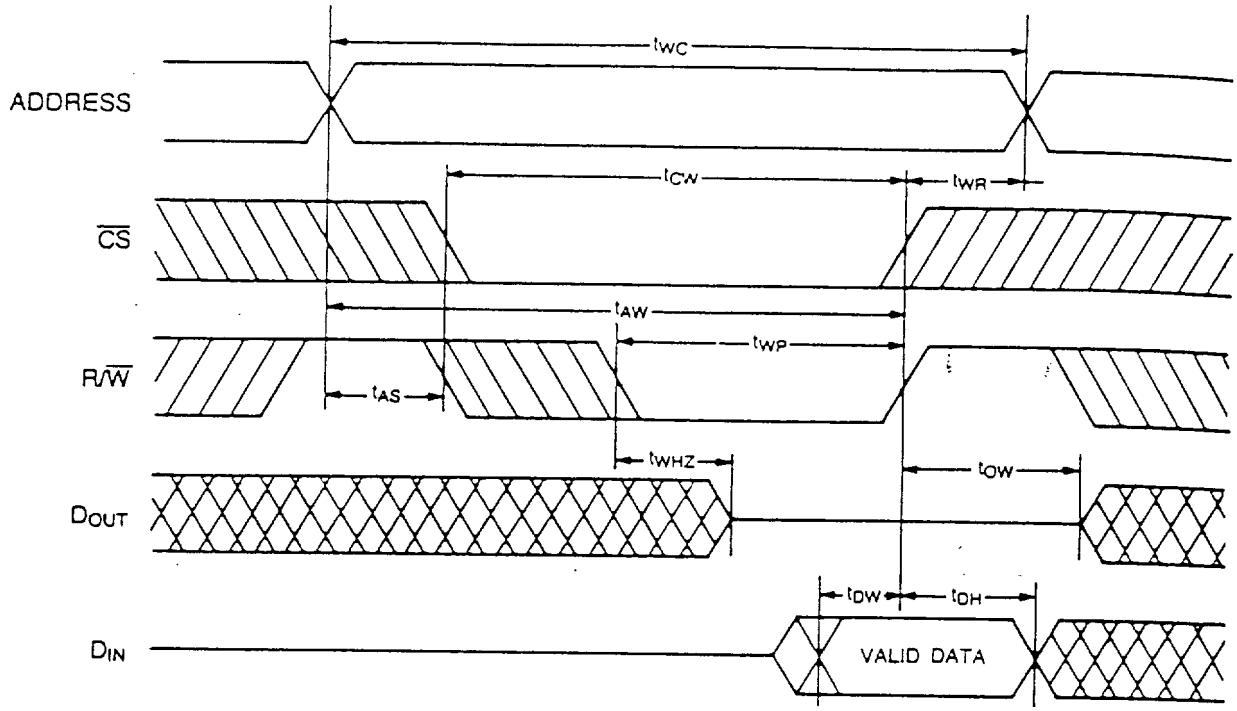


- SW is set to the V_{CC} side when measuring Hi-Z-high and high-Hi-Z of t_{OW} or t_{WHZ}
- SW is set to the V_{SS} side when measuring Hi-Z low and low-Hi-Z of t_{OW} or t_{WHZ}

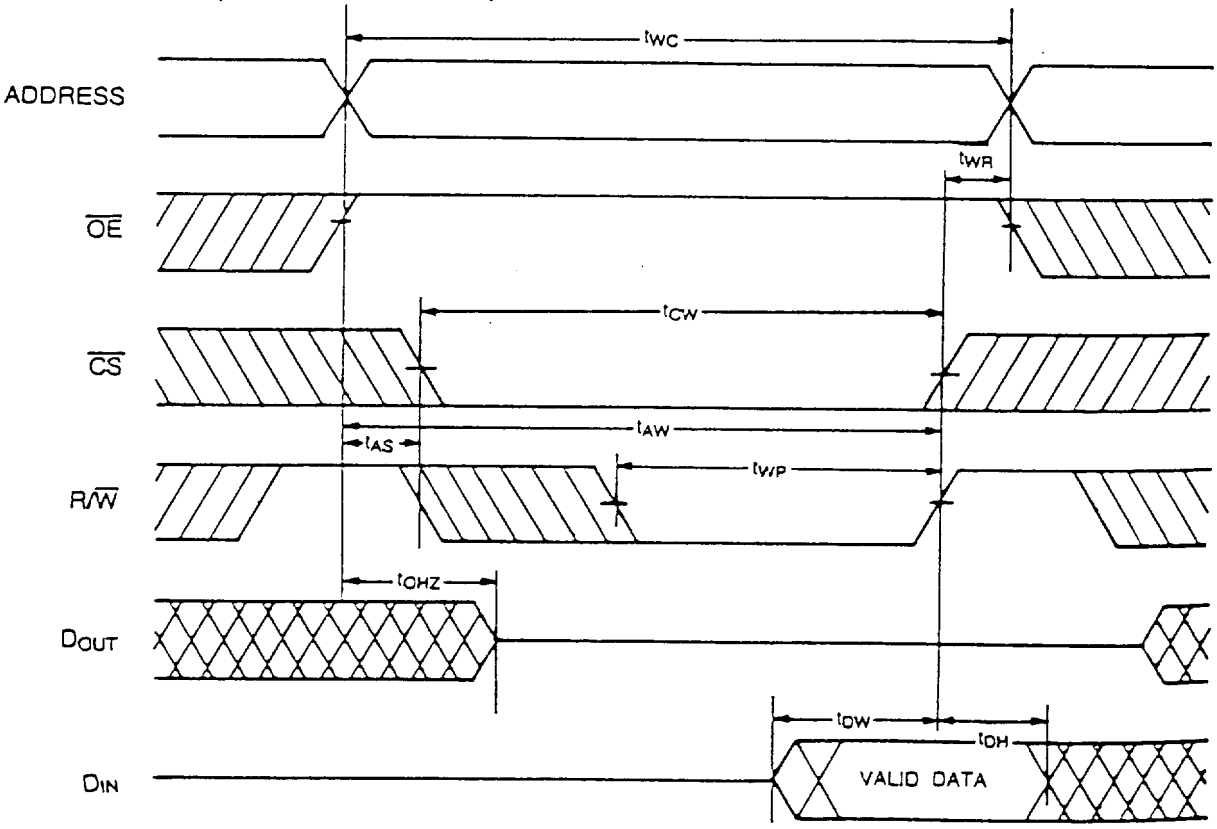
Output turn-on turn-off time



WRITE CYCLE 1 (R/$\overline{W}$ CONTROL, $\overline{OE}$ = LOW)



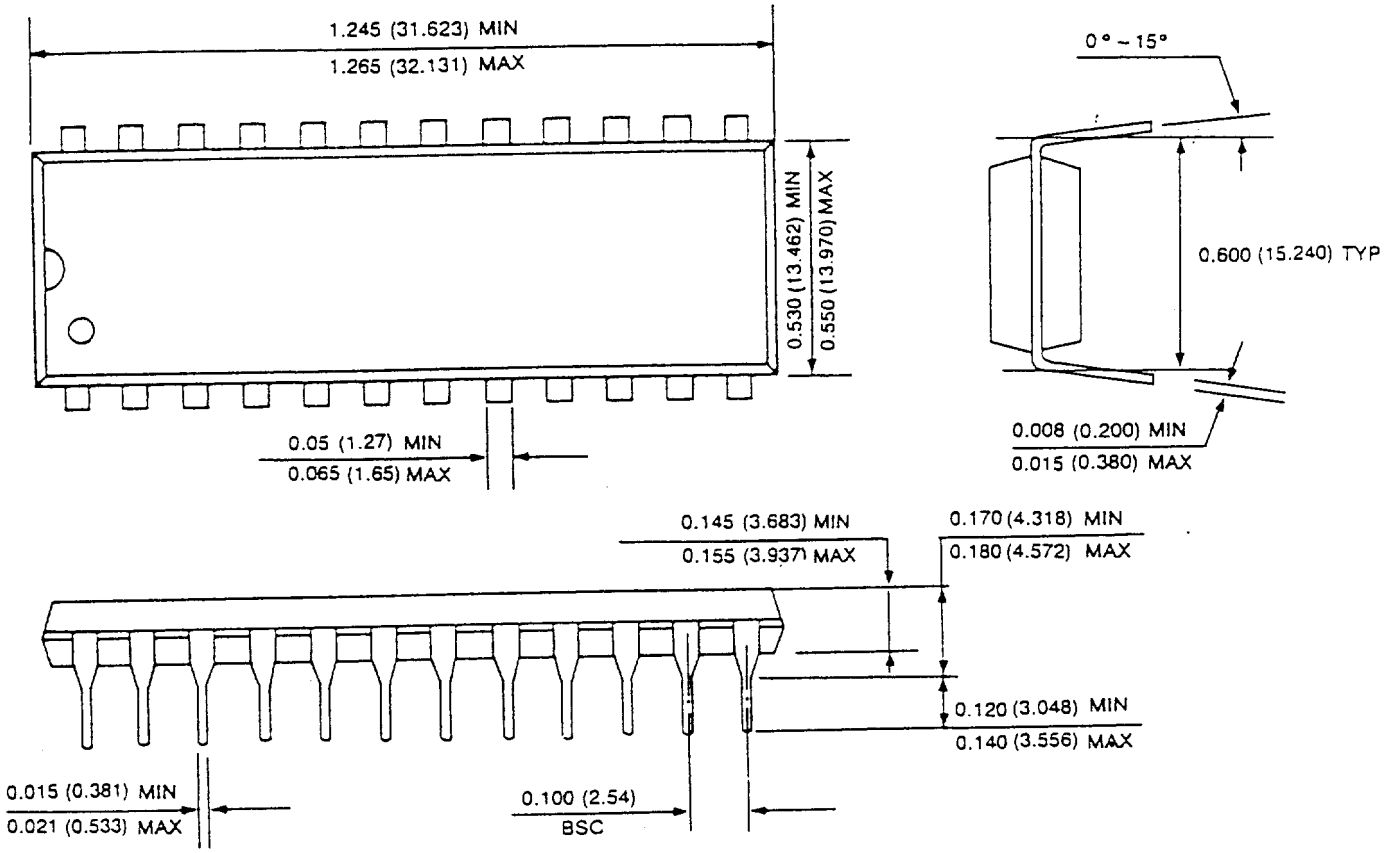
WRITE CYCLE 2 (R/$\overline{W}$ CONTROL)



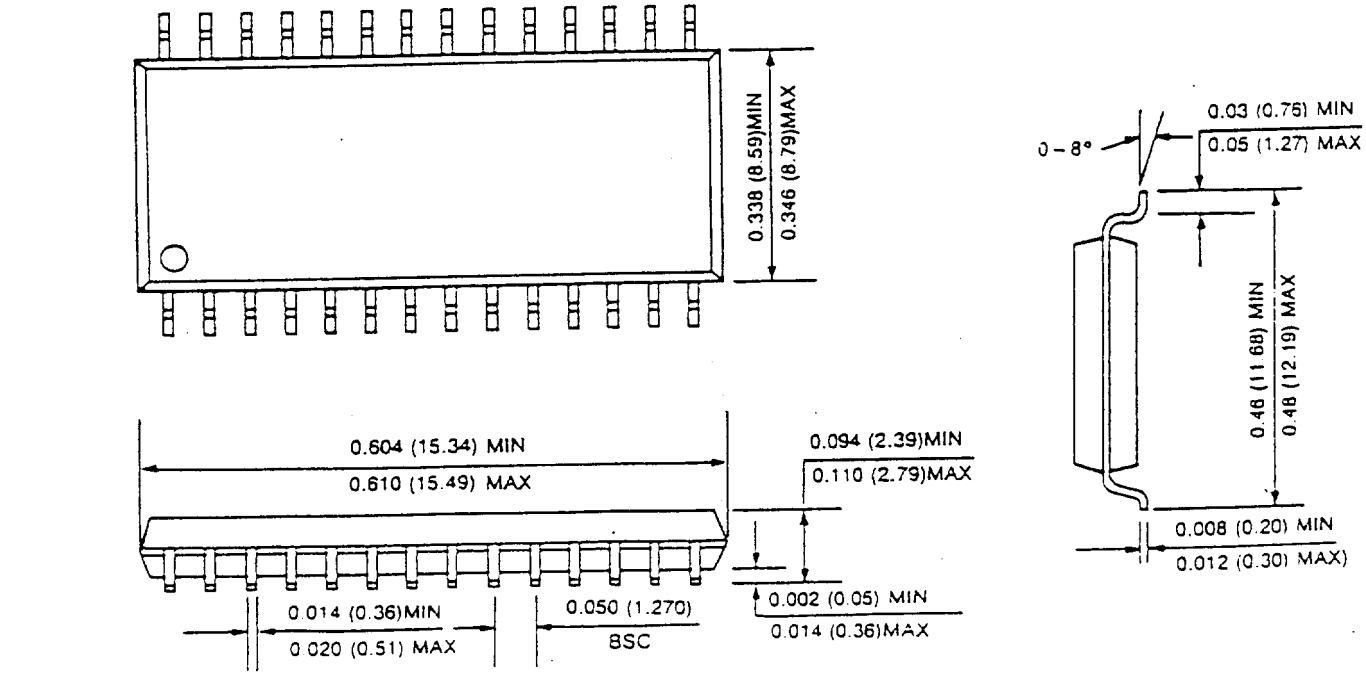
Package Dimensions

Unit: inches (mm)

24 DIP

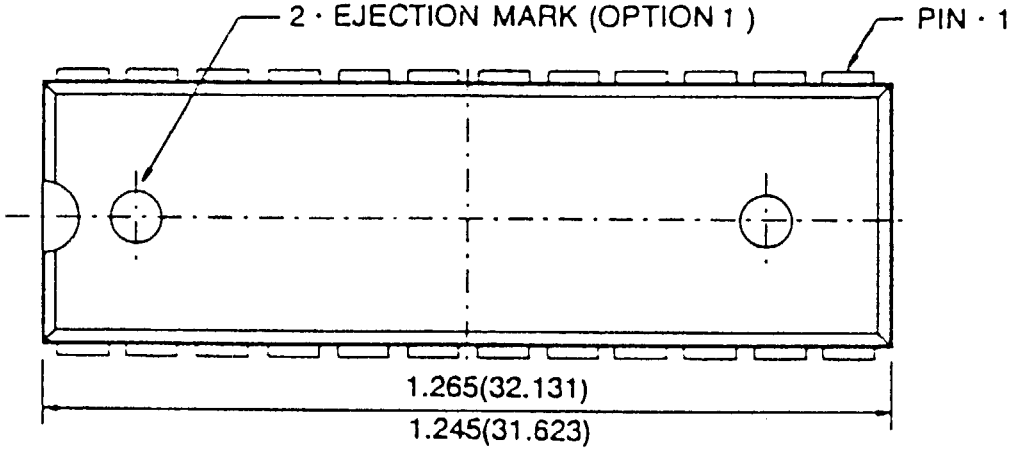


24 SOP

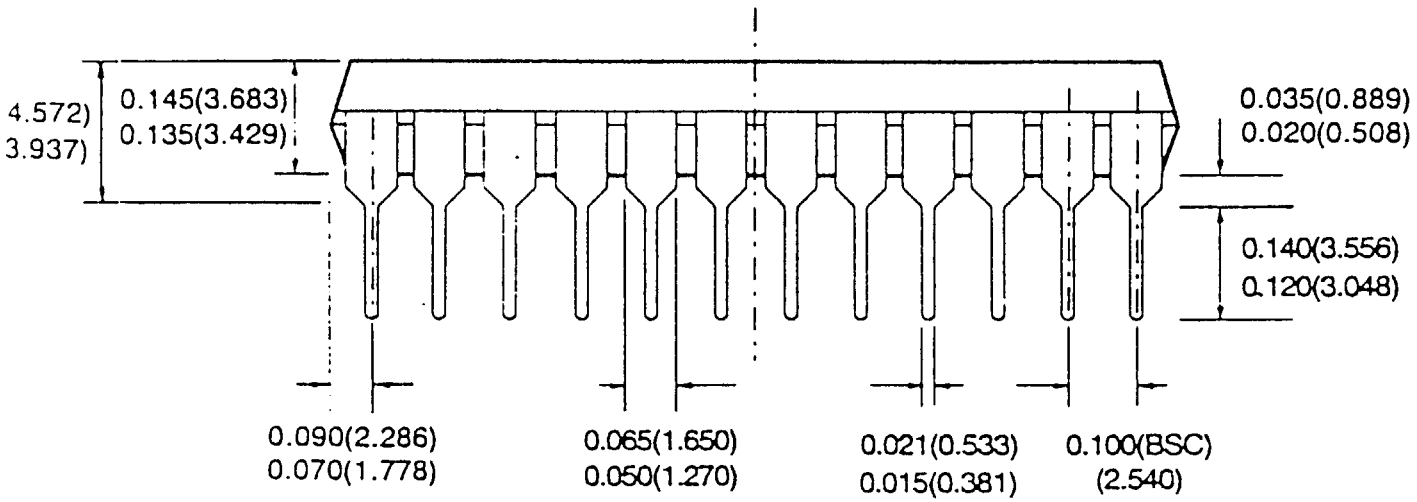


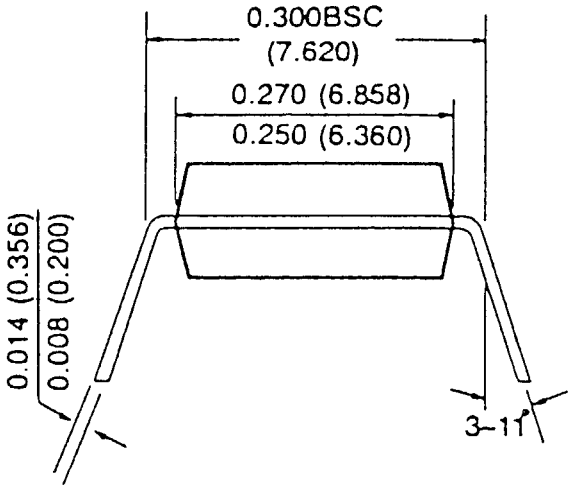
24 SKINNY

UNIT:INCH (mm) MAX/MIN



NOTE
1. LEAD FRAME, COPPER TTT
2. LEAD FINISH, SOLDER PLATED OR SOLDER COATED.
3. BACK EJECTOR PIN MARKED "KOREA"
4. BOTH PACKAGE LENGTH AND WIDTH DO NOT INCLUDE FLASH.
5. CONTROLLING DIMENSION; INCHES (mm)





Capacitance ($f = 1MHz$, $T_A = 25°C$)

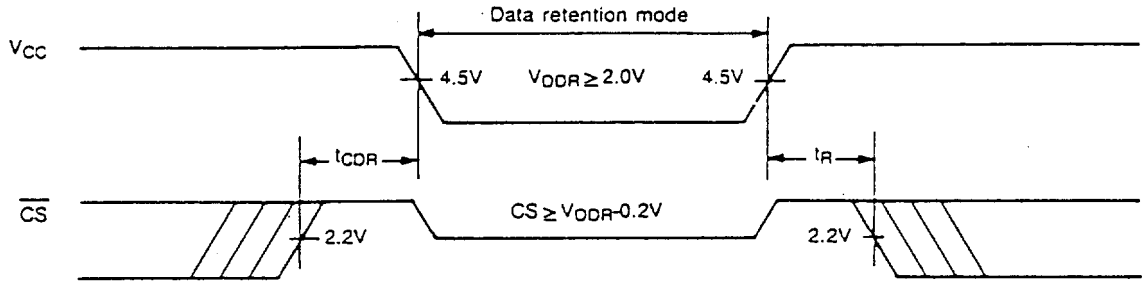
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input Capacitance	$V_I = 0V$		4	6	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O} = 0V$		6	8	pF

Data Retention Characteristics ($T_A = 0 \sim 70°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CCR} - 0.2V$	2.0	—	5.5	V
I_{CCR}	Data Retention Current	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$	—	-	25	μA
t_{CDR}	Chip Select Data Hold Time	Refer to the figure below	0	—	—	ns
t_R	Operation Recovery Time		t_{RC}*	—	—	ns

*t_{RC}: read cycle time

Data retention timing



Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

VRITE CYCLE 3 ($\overline{CS}$ CONTROL, $\overline{OE}$ = LOW)