IMS1203
CMOS High Performance 4K x 1 Static RAM

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 1 Bit Organization
- 25, 35, and 45 nsec Access Times
- 25, 35, and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 18 Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

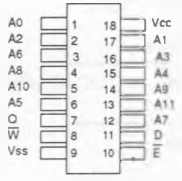
DESCRIPTION

The INMOS IMS1203 is a high performance 4Kx1 CMOS static RAM. The IMS1203 allows speed enhancements to existing 4Kx1 applications with the additional benefit of reduced power consumption.

The IMS1203 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1203 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

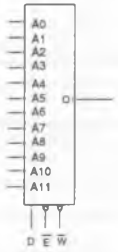
The IMS1203M is a MIL-STD-883 version intended for military applications.

PIN CONFIGURATION

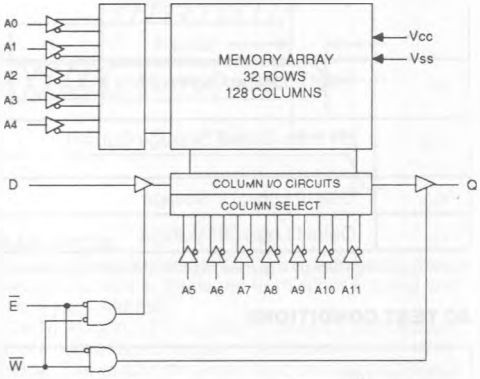


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc POWER
W	WRITE ENABLE	Vss GROUND
D	DATA INPUT	
E	CHIP ENABLE	
Q	DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... −2.0 to 7.0V
Voltage on Q ..... −1.0 to (V_{CC} + 0.5V)
Temperature Under Bias ..... −55°C to 125°C
Storage Temperature ..... −65°C to 150°C
Power Dissipation 1W
DC Output Current 25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc +.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current		80	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\overline{E} \geq V_{IH}$ All other inputs $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		6	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All other inputs at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		13	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ Inputs cycling at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 12mA

Note a: I_{CC} is dependent on output loading and cycle rate. The specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

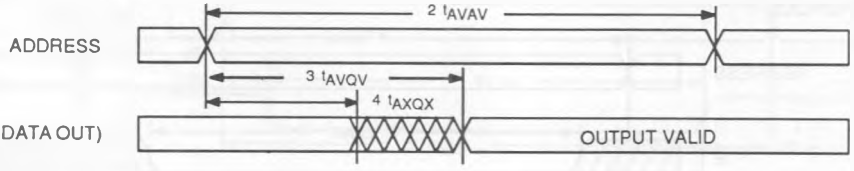
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10%)

READ CYCLE[g]

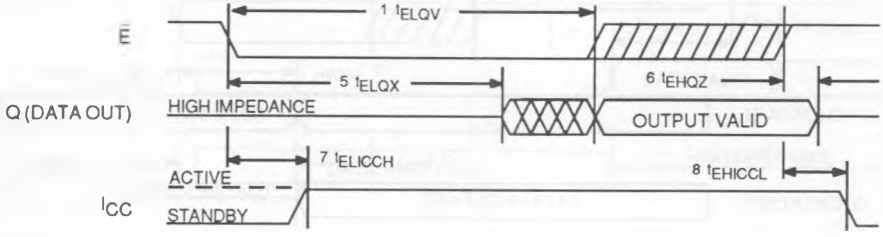
NO.	SYMBOL Standard	SYMBOL Alternate	PARAMETER	1203-25 MIN	1203-25 MAX	1203-35 MIN	1203-35 MAX	1203-45 MIN	1203-45 MAX	UNITS	NOTES
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	30	0	30	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		20		20		20	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



DEVICE OPERATION

The IMS1203 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), a data in (D_{IN}) and a data out (D_{OUT}). The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one memory cell out of 4096. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

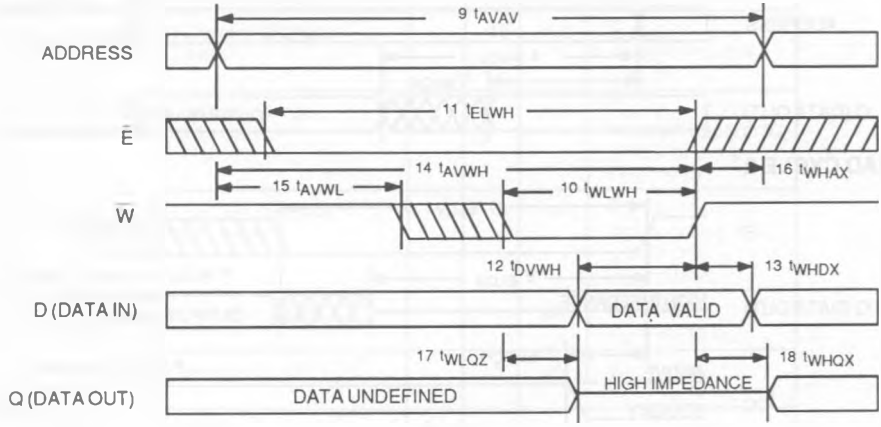
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1203 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to fall. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELOX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLOZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of

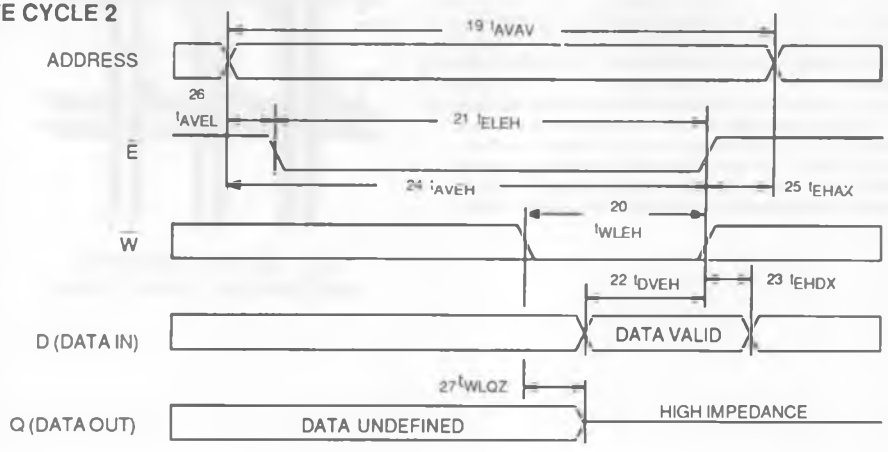
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1203, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1203. The impedance in the decoupling path from the power pin (18) through the decoupling capacitor to the ground pin (9) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1203 have very high frequency

components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

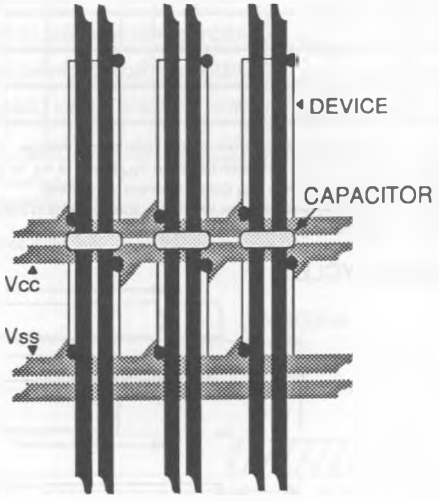
The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

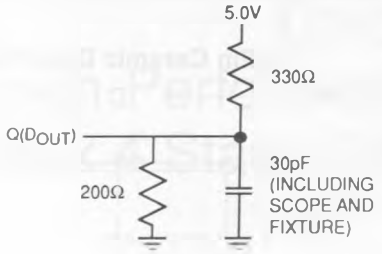
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

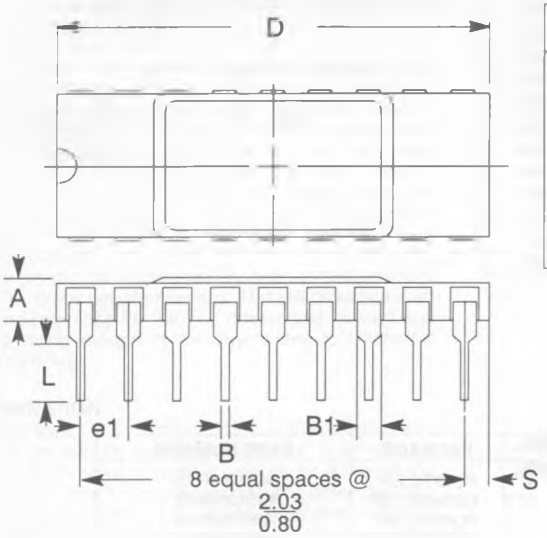
FIGURE 1. OUTPUT LOAD



DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1203	25ns	PLASTIC DIP	IMS1203P-25
	25ns	CERAMIC DIP	IMS1203S-25
	35ns	PLASTIC DIP	IMS1203P-35
	35ns	CERAMIC DIP	IMS1203S-35
	45ns	PLASTIC DIP	IMS1203P-45
	45ns	CERAMIC DIP	IMS1203S-45

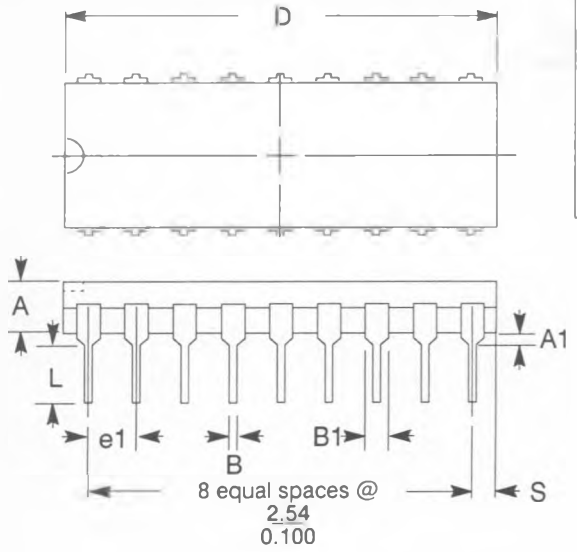
PACKAGING INFORMATION

18 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.085	.010	2.18	.230
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	.900	.011	22.86	.279
E	.310	.010	7.874	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508
S	.005		.127	

18 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.130	.007	3.302	.178
A1	.020	min	.508	min
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Typ
D	.900	.011	22.86	.279
E	.300	.003	7.874	.254
E1	.295	.015	7.620	.076
e1	.100	.010	2.54	.254
eA	330	.020	8.382	.508
L	.135	max	3.429	max
S	.050		.127	