Am9101 Family

256 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

- Low operating power
  125 mW typ.; 290 mW maximum — standard power
  100 mW typ.; 175 mW maximum — low power
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400 mV
- Two chip enable inputs
- Output disable control

GENERAL DESCRIPTION

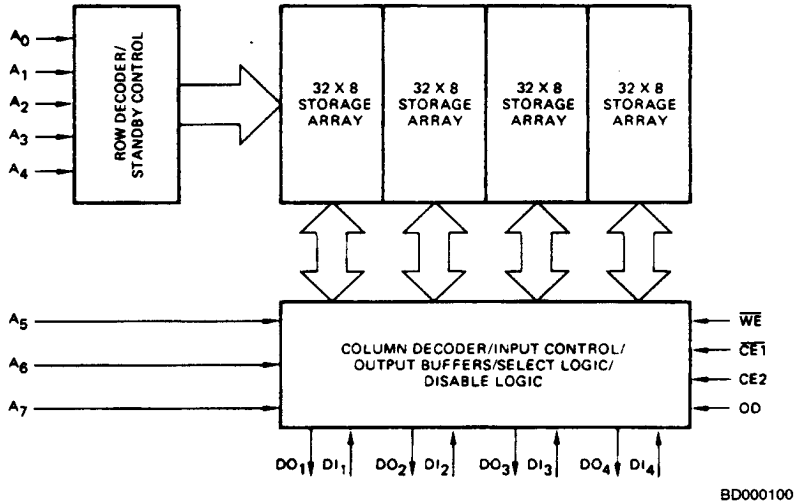
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, Static, Read/Write Random Access Memories. They offer a wide range of access times including versions as fast as 200 ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are fully static and no refresh operations, sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

BLOCK DIAGRAM



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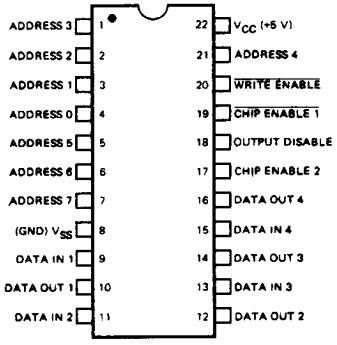
Publication #	Rev.	Amendment
03255	D	/0

Issue Date: May 1986

CONNECTION DIAGRAM
Top View



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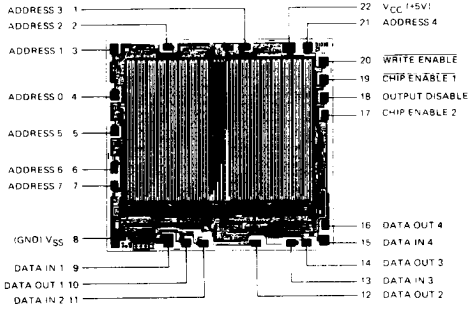
Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT



Die Size 0.132" x 0.131"

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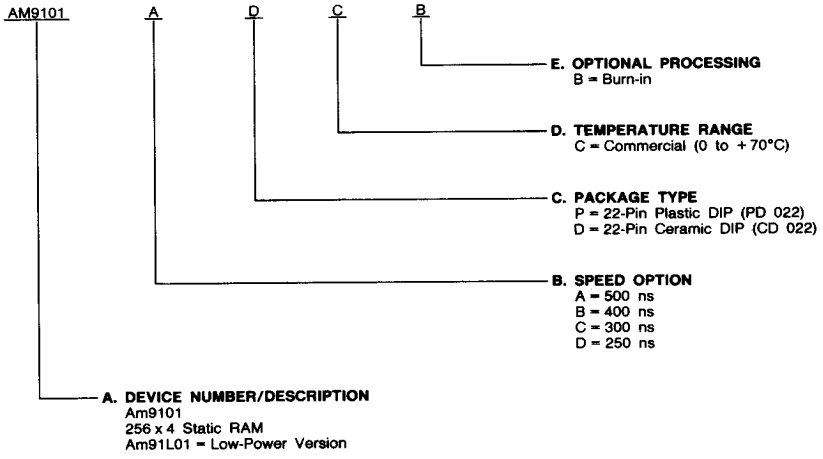
ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9101A	PC, PCB, DC, DCB
AM9101B	
AM9101C	
AM9101D	
AM91L01A	
AM91L01B	
Am91L01C	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

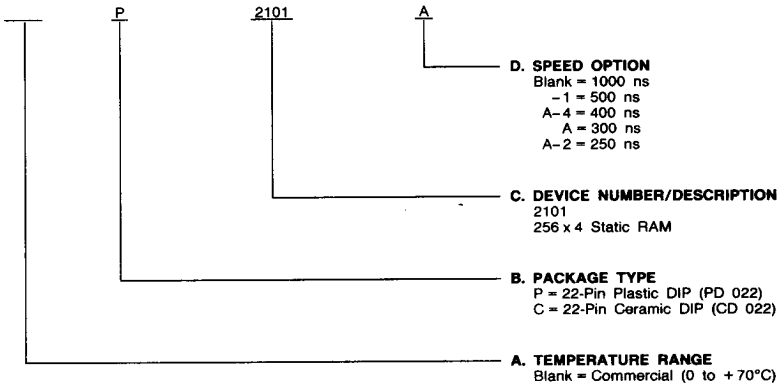
CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability,

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Temperature Range**
B. Package Type
C. Device Number
D. Speed Option



Valid Combinations		
P, C	2101	-1, A-4, A, A-2

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_7$ Addresses (Input)
The 8-bit field presented at the address inputs selects one of the 256 memory locations to be read from — or written into — via the Data Input/Output lines.

$DI_1 - DI_4$ Data In Lines (Input)
The inputs whose states represent the data to be stored in memory.

$DO_1 - DO_4$ Data In Lines (Output)
The outputs whose states represent the data to be stored in memory.

$\overline{CE1}$, CE2 Chip Enable Signals (Input)
Read and Write cycles can be executed only when $\overline{CE1}$ is LOW and CE2 is HIGH.

$\overline{WE}$ Write Enable (Input, Active LOW)
Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

OD Output Disable (Input)
Read cycles can be executed only when OD is LOW.

FUNCTIONAL DESCRIPTION

Applications

Refer to Figure 1 for Memory System information.

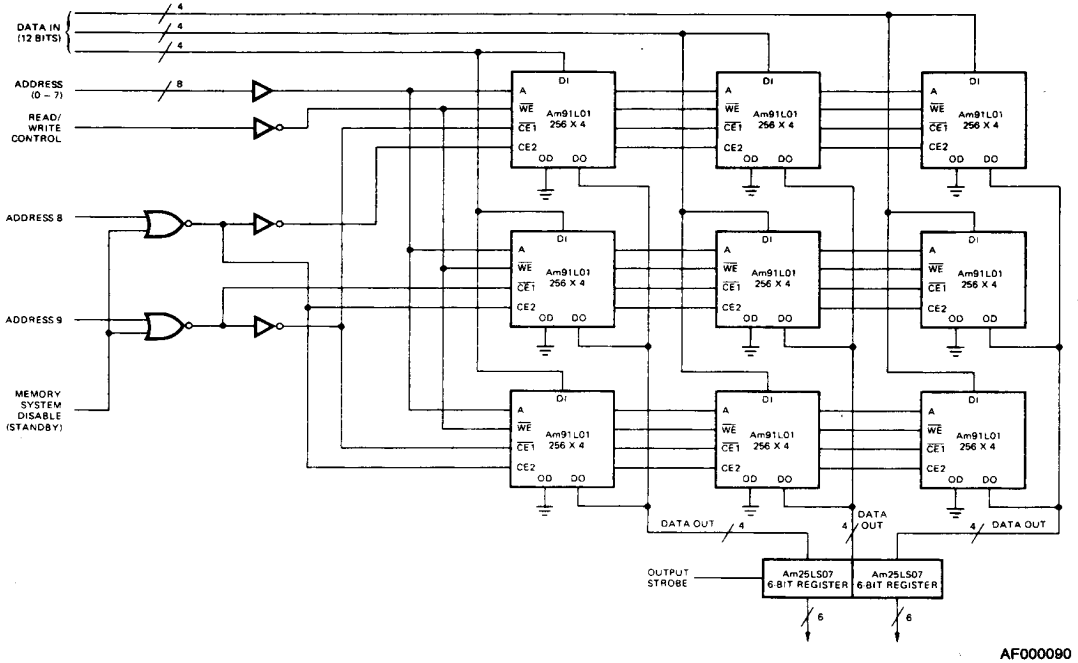


Figure 1. Memory System 768 Words by 12 Bits Per Word

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +7.0 V
DC Layout Voltage ..... −0.5 V to +7.0 V
Power Description ..... 1.0 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Am9101/ Am91L01 Min.	Am9101/ Am91L01 Max.	Am2101 Min.	Am2101 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −200 μA		2.4				V
			I_{OH} = −150 μA				2.2		
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 3.2 mA			0.4			V
			I_{OL} = 2.0 mA					0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	V
I_{LI}	Input Load Current	V_{CC} = Max., 0 ≤ V_{IN} ≤ V_{CC}				10		10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}}$ = V_{IH}	V_O = V_{CC}	C devices		5.0		15	μA
				M devices		10			
			V_O = 0.4 V			−10		−50	
I_{CC1}	Power Supply Center	Data Out Open V_{CC} = Max. V_{IN} = V_{CC}	T_A = 25°C (Note 3)	Am9101A/B		50			mA
				Am9101/C/D/E		55			
				Am91L01A/B		31			
				Am91L01C/D/E		34			
				Am2101				60	
			T_A = 0°C (C devices only)	Am9101A/B		55			
				Am9101C/D/E		60			
				Am91L01A/B		33			
				Am91L01C/D/E		36			
				Am2101				70	
			T_A = −55°C (M devices only)	Am9101A/B		60			
				Am9101C/D/E		65			
				Am91L01A/B		37			
				Am91L01C/D/E		40			
				Am2101					
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{IN} = 0 V (Note 3)				9		9	pF
C_O	Output Capacitance	T_A = 25°C, f = 1 MHz, V_O = 0 V (Note 3)				12		12	

Notes: 1. Absolute maximum ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Guaranteed by characterization data. Data will be updated upon any process or design change which affects this parameter.
4. Test conditions assume signal transition times of 10 ns or less. Output load equals 1 TTL gate + 100 pF. Input signal timing reference level = 1.5 V, with input pulse levels of 0 to 3.0 V. Data output timing reference levels = 0.8 and 2.0 V.
5. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

*See the last page of this spec for Group A Subgroup Testing information.

STANDBY OPERATING CONDITIONS over temperature range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	T_A = 0°C, All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L01		11	25	mA
				Am9101		13	31	
			V_{PD} = 2.0 V	Am91L01		13	31	
				Am9101		17	41	
		T_A = −55°C, All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L01		11	28	mA
				Am9101		13	34	
			V_{PD} = 2.0 V	Am91L01		13	34	
				Am9101		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts

Power-Down Standby Operation

The Am9101/AM91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5 – 2.0 volts (see table and graph). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

To ensure that the output of the device is in a high-impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

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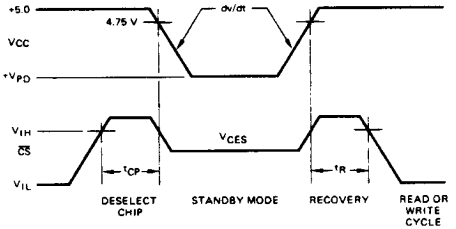
TYPICAL DC AND AC CHARACTERISTICS



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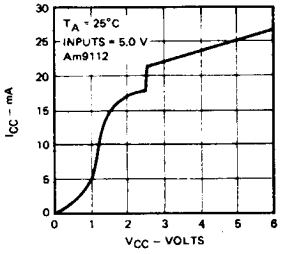
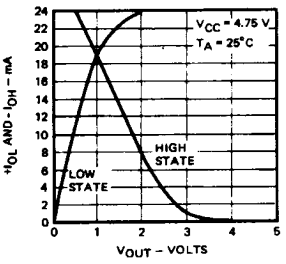
Typical Power Supply Current Versus Voltage



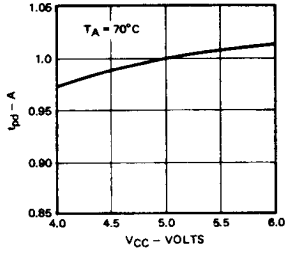
OP000460

Typical Output Current Versus Voltage



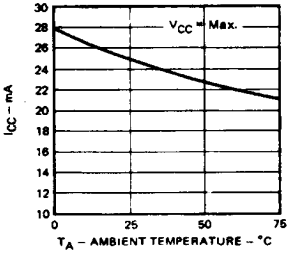
OP001060

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



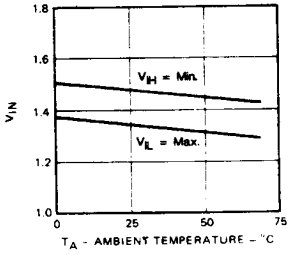
OP000100

Typical Power Supply Current Versus Ambient Temperature



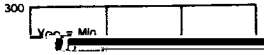
OP001070

Typical V_{IN} Limits Versus Ambient Temperature



OP001030

Typical t_A Versus Ambient Temperature



Typical t_A Versus C_L

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 4)*

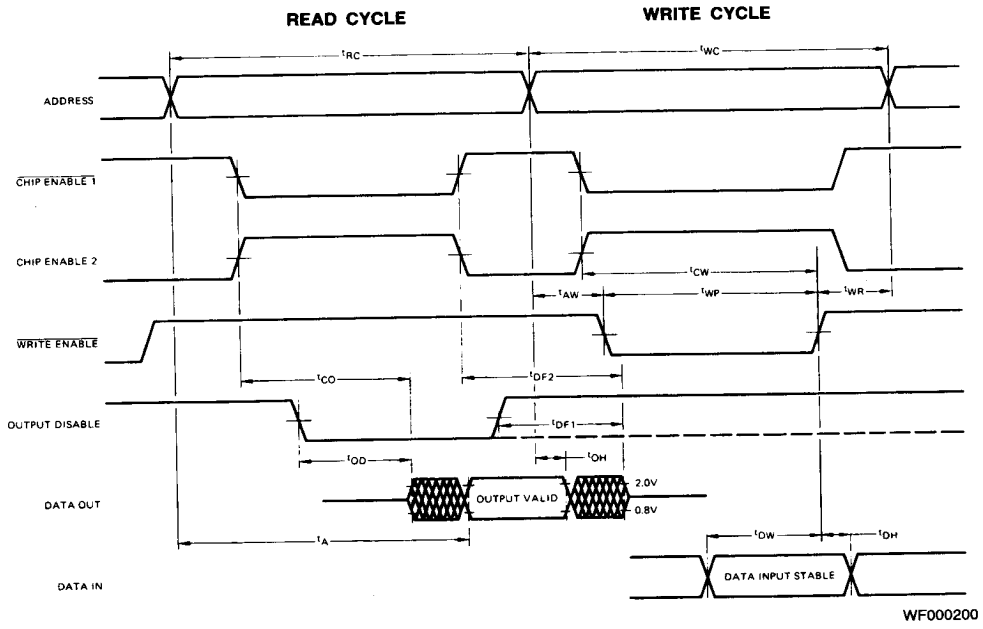
No.	Parameter Symbol	Parameter Description	Am2101		Am2101-2		Am2101-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	1000		650		500		ns
2	t_A	Access Time		1000		650		500	ns
3	t_{CO}	Chip Enable to Output ON Delay (Note 5)		800		400		350	ns
4	t_{OD}	Output Disable to Output ON Delay		700		350		300	ns
5	t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		ns
6	t_{DF1}	Output Disable to Output OFF Delay (Note 3)	0	200	0	150	0	150	ns
7	t_{DF2}	Chip Enable to Output OFF Delay (Note 3)	0	200	0	150	0	150	ns
8	t_{WC}	Write Cycle Time	1000		650		500		ns
9	t_{AW}	Address Set-up Time	150		150		100		ns
10	t_{WP}	Write Pulse Width	750		400		300		ns
11	t_{CW}	Chip Enable Set-up Time (Note 5)	900		550		400		ns
12	t_{WR}	Address Hold Time	50		50		50		ns
13	t_{DW}	Input Data Set-up Time	700		400		280		ns
14	t_{DH}	Input Data Hold Time	100		100		100		ns

No.	Parameter Symbol	Parameter Description	Am9101A Am91L01A		Am9101B Am91L01B		Am9101C Am91L01C		Am9101D		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	500		400		300		250		ns
2	t_A	Access Time		500		400		300		250	ns
3	t_{CO}	Chip Enable to Output ON Delay (Note 5)		200		175		150		125	ns
4	t_{OD}	Output Disable to Output ON Delay		175		150		125		100	ns
5	t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		ns
6	t_{DF1}	Output Disable to Output OFF Delay	5.0	125	5.0	100	5.0	100	5.0	75	ns
7	t_{DF2}	Chip Enable to Output OFF Delay	10	125	10	125	10	100	10	100	ns
8	t_{WC}	Write Cycle Time	500		400		300		250		ns
9	t_{AW}	Address Set-up Time	20		20		20		20		ns
10	t_{WP}	Write Pulse Width	225		200		175		150		ns
11	t_{CW}	Chip Enable Set-up Time (Note 5)	175		150		125		100		ns
12	t_{WR}	Address Hold Time	0		0		0		0		ns
13	t_{DW}	Input Data Set-up Time	150		125		100		85		ns
14	t_{DH}	Input Data Hold Time	15		15		15		15		ns

See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



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GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
V_{PD}	1, 2, 3
I_{PD}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11
2	t_A	7, 8, 9, 10, 11
3	t_{CO}	7, 8, 9, 10, 11
4	t_{OD}	7, 8, 9, 10, 11
5	t_{OH}	7, 8, 9, 10, 11
8	t_{WC}	7, 8, 9, 10, 11
9	t_{AW}	7, 8, 9, 10, 11
10	t_{WP}	7, 8, 9, 10, 11
11	t_{CW}	7, 8, 9, 10, 11
12	t_{WR}	7, 8, 9, 10, 11
13	t_{DW}	7, 8, 9, 10, 11
14	t_{DH}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.